Temperature-independent switching rates for a random telegraph signal in a silicon metal–oxide–semiconductor field-effect transistor at low temperatures

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We have observed discrete random telegraph signals (RTSs) in the drain voltages of three, nominally $1.25\,\mu\text{m}\times 1.25\,\mu\text{m}$, enhancement-mode *p*-channel metal–oxide–semiconductor transistors operated in strong inversion in their linear regimes with constant drain-current and gate-voltage bias, for temperatures ranging from 4.2 to 300 K. The switching rates for all RTSs observed above 30 K were thermally activated. The switching rate for the only RTS observed below 30 K was thermally activated above 30 K but temperature independent below 10 K. This response is consistent with a crossover from thermal activation to tunneling at low temperatures. Implications are discussed for models of change exchange between the Si and the near-interfacial SiO_2. [S0003-6951(00)01822-2]

Metal–oxide–semiconductor field-effect transistors (MOSFETs) often exhibit relatively large levels of low-frequency ($1/f$) noise.[1,2] Much evidence suggests that this noise is related to the capture and emission of charge carriers by localized defects at or near the Si/SiO_2 interface.[2–6] Under constant current bias, the drain voltages of small gate-area devices often show random switching between two discrete levels, apparently from the capture and emission of individual charge carriers.[2,7–11] Such random telegraph signals (RTSs),[12] observed in small gate-area devices, superpose to give $1/f$ noise in larger devices.[2,7] Thus, the study of RTSs in MOSFETs is helpful in understanding the origins of $1/f$ noise and defects near the Si/SiO_2 interface. In particular, the dominant type of charge exchange between the Si and defects in the near-interfacial oxide remains an open question in models of MOS performance, long-term reliability, and radiation response.

There have been many observations of random telegraph signals in small MOSFETs.[2,7–11] In past work, switching rates have been thermally activated, often with different activation energies for capture and emission. Ralls *et al.*[7] first recognized that these phenomena cannot be due to simple capture and emission of charge carriers from a single trap of fixed energy. The data suggest that capture and/or emission are accompanied by lattice relaxation. Though thermally activated behavior is consistently observed at higher temperatures, one might expect to see temperature-independent behavior consistent with tunneling events at sufficiently low temperatures.[7,9] Such a crossover from thermal activation to configurational tunneling has been observed for RTSs in tunnel junctions.[13]

We have investigated the noise in three $\sim 1.25\,\mu\text{m}\times 1.25\,\mu\text{m}$, *p*-channel, enhancement-mode MOSFETs mounted in 24-pin dual in-line packages at temperatures down to 4.2 K. The devices have a gate-oxide thickness of 18 nm and were fabricated using radiation-hardened technology,[14] and therefore, exhibit a low density of near-interfacial oxide (border) traps.[6] Devices were *not* irradiated prior to noise measurement. Threshold voltages were approximately -1.0 V at $\sim$300 K and -1.5 V at $\sim$10 K. Temporal fluctuations δV_d in the source–drain voltage V_d were observed with devices operated in their linear regimes with fixed gate-source voltage V_g and drain current I_d. The measurement circuit is similar to that used to characterize $1/f$ noise in larger devices.[5] The measurement bandwidth was 0.03 Hz to 30 kHz. For these devices, the statistical properties of the RTSs were very reproducible, even after many days and temperature cycles.

For each device it was possible to find a range of temperatures and gate voltages for which the drain voltage was observed to randomly switch between two discrete levels, designated as V_{up} and V_{dn}, similar to RTSs reported by others.[2,7–11] We have characterized six RTSs for temperatures above 30 K where thermally activated switching rates are observed. The properties of five of these have been described in a prior study.[15] Here, we describe the single RTS that was observable for temperatures T both below and above 30 K. The presence or absence of a RTS in a particular temperature-bias window is determined by both the position and the energy of the trap,[6–9] so it is not surprising that only a limited number of defects might have the proper positions and/or energies to be observable in the range accessible in these MOSFET experiments.

The RTS examined here was characterized by its voltage change $\Delta V \equiv V_{\text{up}} - V_{\text{dn}}$ and the mean times τ_{up} and τ_{dn} spent in the ''up'' and ''down'' voltage states. We found the data to be consistent with the idea that the high-resistance state

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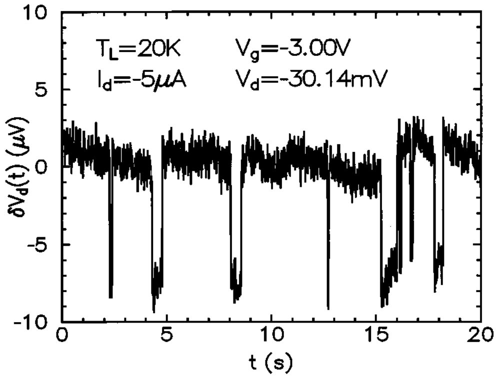

FIG. 1. Time trace of the fluctuation in the drain voltage at a lattice temperature of 20 K. For this *p*MOS device, a more negative voltage corresponds to a higher-resistance state.

V_{dn} was associated with the trapping of a single-charge carrier. Thus, we identify the mean time in the high-resistance state (τ_{dn} in state V_{dn}) as the emission time τ_e for the trap, i.e., the mean time a captured charge carrier spends in the trap before it is emitted. Similarly, we identify the mean time in the low-resistance state (τ_{up} in state V_{up}) as the capture time τ_c. Figure 1 shows a typical time trace of the drain-voltage fluctuation $\delta V_d(t) \equiv V_d(t) - \langle V_d \rangle$. This particular measurement was recorded for $T = 20\,\mathrm{K}$, $I_d = -5\,\mu\mathrm{A}$, and $V_g = -3.00\,\mathrm{V}$ (~1.5 V above threshold). The measured (average) drain voltage was $\langle V_d \rangle = -30.14\,\mathrm{mV}$. As indicated in Fig. 1, the RTS is more often in the ''up'' state than in the ''down'' state, corresponding to a normally empty trap. For this RTS we find $\Delta V = (8 \pm 1)\,\mu\mathrm{V}$, $\tau_e = (0.44 \pm 0.09)\,\mathrm{s}$, $\tau_c = (1.56 \pm 0.36)\,\mathrm{s}$, and the duty-cycle $\eta \equiv \tau_c/(\tau_c + \tau_e) = 0.78$. As shown below, RTS switching rates can depend very strongly on gate bias. At all temperatures the capture rate increases and the emission rate decreases with more negative gate bias. Roughly a decade change in both rates occurs for a 10 mV change in V_g at 4 K and a 20 mV change in V_g at 30 K. To observe a RTS at any temperature, it is often necessary to retune the gate voltage slightly to bring the rates into the experimental time window.

To determine the temperature dependence of the switching rates the device was biased at constant drain current (-15 μA), and gate voltage (-3.00 V) and measurements were performed at temperatures ranging from 4.2 to 35 K. Figure 2 shows Arrhenius plots of τ_c and τ_e for the higher-

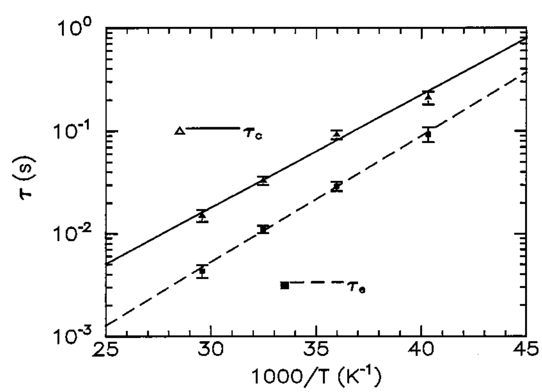

FIG. 2. Arrhenius plot showing the thermally activated behavior of both the mean capture (triangle) and emission (square) times of the RTS for temperatures above 20 K.

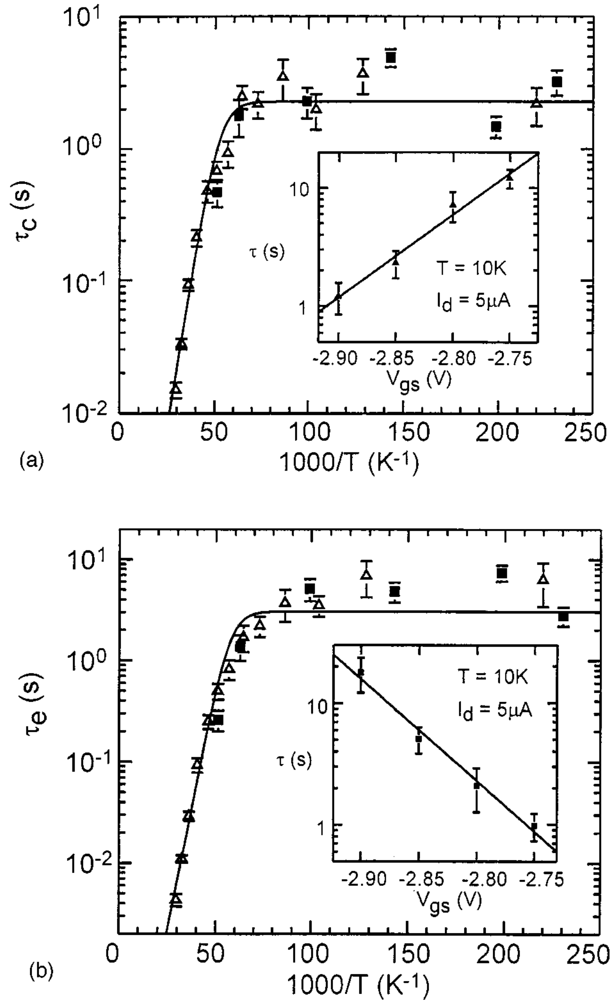

FIG. 3. Arrhenius plot showing the temperature dependence of the mean capture time (a) and emission time (b) for a RTS for 4.2–30 K. The open triangles represent data measured with $V_g = -3.00\,\mathrm{V}$ and $I_d = -15\,\mu\mathrm{A}$, while the solid squares represent data measured with $V_g = -2.85\,\mathrm{V}$ and $I_d = -5\,\mu\mathrm{A}$. The line represents the theory with three adjustable parameters obtained using a weighted nonlinear least-squares fit to the triangle data. Insets show the strong voltage dependence of the RTSs.

temperature measurements, i.e., for $T = 25$–$35\,\mathrm{K}$. Both capture and emission times vary by more than an order of magnitude in this narrow range of temperature, in a manner consistent with thermal activation. Linear least-square fits yield activation energies $E_c = (23 \pm 2)\,\mathrm{meV}$ and $E_e = (26 \pm 1)\,\mathrm{meV}$.

Switching times for the full range of temperatures are shown in Fig. 3. Data represented by open triangles were measured with $I_d = -15\,\mu\mathrm{A}$ and $V_g = -3.00\,\mathrm{V}$. The solid curves represent a theoretical fit to the triangle data with three adjustable parameters (see below). Figures 3(a) and 3(b) indicate that both the mean capture and emission times are independent of T at low temperatures and increase rapidly with T at high temperatures. The strong gate-voltage dependence of the RTSs is emphasized in the insets. To model the switching response, we assume that both the capture and emission rate may be represented by the sum of two rates, one being thermally activated and the other being temperature independent. Specifically, we write

$$\frac{1}{\tau_\alpha} = \frac{1}{\tau_{\alpha,1}} + \frac{1}{\tau_{\alpha,2}}, \tag{1}$$

where α = capture or emission, $\tau_{\alpha,1}$ is temperature independent, and $\tau_{\alpha,2}$ is thermally activated, i.e.,

$$\tau_{\alpha,2}=\tau_{\alpha,2}(\mathbf{T})=\tau_{a,0}\exp(\mathbf{E}_\alpha/\mathbf{k}_b\mathbf{T}), \tag{2}$$

k_b is the Boltzmann constant, and $\tau_{\alpha,0}$ and E_α are the temperature-independent attempt time and activation energy, respectively. Thus

$$\tau_\alpha(\mathbf{T})=\frac{\tau_{\alpha,1}\tau_{\alpha,0}\exp(\mathbf{E}_\alpha/\mathbf{k}_b\mathbf{T})}{\tau_{\alpha,1}+\tau_{\alpha,0}\exp(\mathbf{E}_\alpha/\mathbf{k}_b\mathbf{T})}. \tag{3}$$

The solid curve in Fig. 3(a) (mean capture time) was obtained using a weighted nonlinear least-squares fit of Eq. (1) to the triangle data, with weighting inversely proportional to the square of the uncertainty in the measured times. A minimum in the chi-square per degree of freedom of 2.3 was obtained for $\tau_{c,1}=(2.3\pm0.4)$ s, $\tau_{c,0}=(5\pm3)$ μs, and $E_c=(18\pm2)$ meV. For Fig. 3(b) (mean emission time) the solid curve was obtained similarly, also yielding a value of the chi-square per degree of freedom of 2.4 for $\tau_{e,1}=(3.1\pm0.6)$ s, $\tau_{e,0}=(9\pm4)$ μs, and $E_e=(19\pm2)$ meV.

Care is required to ensure the crossover in behavior in Fig. 3 is not an artifact of the measurement technique. Heating effects are especially important to rule out. This could be a problem if the charge carriers are not in thermal equilibrium with the lattice. That is, while the lattice is being cooled from 20 to 4.2 K, the holes could remain at essentially constant temperature due to drain-current-induced heating. In that case, the lack of temperature dependence in Fig. 3 would be a result of heating, instead of a transition from thermally activated to tunneling charge exchange. We reject this explanation due to the following simple argument. If heating were a significant factor in these measurements, we would expect the measured capture and emission rates to depend strongly upon the power dissipated in the channel. To test this, we performed additional measurements for $I_d=-5$ μA and $V_g=-2.85$ V, plotted as the solid squares in Fig. 3 above. Because the channel resistance does not depend strongly on the gate voltage, these conditions correspond to roughly a factor of 9 times lower-power dissipation than for the earlier measurements and should, therefore, be much less sensitive to heating effects. Within experimental error, the two sets of data agree in Fig. 3. Therefore, it seems unlikely that the temperature-independent rates are an experimental artifact associated with carrier heating.[16,17]

We believe that the transition from thermally activated to temperature-independent switching rates illustrated in Fig. 3 may be associated with a lattice relaxation mechanism similar to that observed in metal–insulator–metal tunnel junctions.[13] Capture and emission of carriers in the near-interfacial SiO_2 are mediated by lattice relaxation. For defects at a suitable position and energy level, charge exchange between the Si and the SiO_2 can proceed via a thermally activated process at higher temperatures and a configurational tunneling process at lower temperatures.[7,9,18] This result appears to contrast with a recent report of temperature-independent hysteresis attributed to the tunnel exchange of electrons with border traps in MOS capacitors reported by Bhat and Saraswat[19] over a temperature range of 293–473 K. Instead, these results and other RTS studies in MOSFETs at higher temperatures[2,7–11] are consistent with the idea that exchange of carriers between the Si and the near-interfacial SiO_2 via a pure tunneling process is significantly less probable than exchange via a thermally activated process, except perhaps at very low temperatures.

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[16] The relative importance of lattice versus carrier temperature is interesting to consider further. Jackel and co-workers have performed experiments to separate effects of electron and lattice temperature on switching rates of a RTS in a narrow *n*-channel MOSFET. They found that the electron capture rate depended on both lattice and electron temperatures while the emission rate depended only upon lattice temperature (see Ref. 17). This experiment is frequently quoted in support of trapping models, but we are unaware of attempts to duplicate it with other samples. In the future, it would be interesting to separate out the effects associated with lattice and carrier temperatures for other RTSs in MOSFETs or other physical systems.
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