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RANDOM TELEGRAPH SIGNALS IN SMALL GATE-AREA P-MOS TRANSISTORS*

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ABSTRACT

We report the observation of random telegraph signals (RTS) in the channel resistances of nominally 1.25 µm x 1.25 µm, enhancement-mode pMOS transistors fabricated using the AT&T 1-µm radiation hardened technology. Devices were operated in strong inversion in the linear regime. Measurements, performed for temperatures ranging from 77 to 300 K and various gate voltages, show that capture and emission times are both thermally activated and that the capture time depends strongly on the gate voltage. Results suggest that the unfilled trap is charged and that, after capturing a hole, the trap relaxes to a lower energy. Basic features of a model are discussed.

EXPERIMENTAL RESULTS AND DISCUSSION

Metal-oxide-semiconductor (MOS) transistors are known to exhibit relatively large levels of low-frequency 1/f noise.[1] Much evidence now suggests that this noise is related to the capture and emission of charge carriers by localized defects at or near the Si/SiO_2 interface.[2,3,4] The drain voltage of very small gate-area devices, especially at low temperatures, shows random switching between two discrete levels, apparently arising from the capture and emission of a single charge carrier.[2,5,6,7,8] Such random telegraph signals (RTS), observed in small gate-area devices, have been shown to superpose to give 1/f noise in larger area devices.[2] Thus, information gained from the study of RTS's in MOSFETs should be helpful in understanding the origins of 1/f noise in these devices.

We have investigated six RTS's in two relatively small gate-area ($\approx$ 1.25 µm x 1.25 µm) p-channel, enhancement mode MOS transistors operated in strong inversion. Devices have an oxide thickness of 18 nm and were fabricated using the AT&T 1-µm radiation hardened technology.[9] To our knowledge these devices have the lowest defect-density and are the most radiation-tolerant of any devices used for such studies. Temporal fluctuations ($\delta V_d(t)$) in the drain voltage (V_d) were observed when devices were operated in their linear regimes with fixed gate voltage (V_g) and drain current (I_d); the source lead was grounded during all measurements.[10] The measurement conditions were similar to those we have used previously for noise measurements on large area devices.[3] Measurements were performed for sample temperatures (T) between 77 and 300 K and effective gate-voltages (V_g-V_{th}) ranging from -200 mV to -2 V, where V_{th} is the threshold voltage. The measurement bandwidth was from 0.03 Hz to 30 kHz and typically -100 mV < V_d < 0. For these devices, RTS's were very reproducible even after many days and multiple temperature cycles.

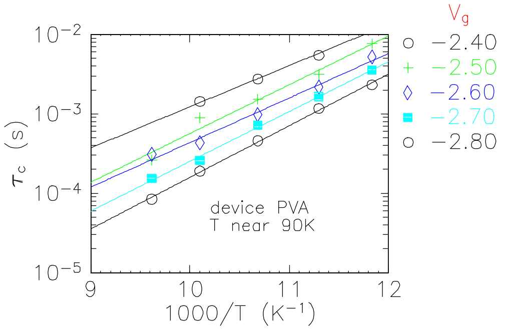

Figure 1. Semilog plot of capture time versus inverse temperature at fixed gate voltage.

For each device it was possible to find a range in T and V_g for which V_d was observed to randomly switch between two discrete levels, similar to behavior reported by others.[2,5-8] The drain-voltage switching scaled with the I_d indicating switching in the channel resistance, $\delta R_{ch} = \delta V_d/I_d$. No attempt was made to use the drain-voltage dependence to locate the trap along the channel.[8] The RTS's were characterized by their resistance changes ΔR_{ch} and their mean times in the "high-" and "low-resistance" states. We found the dependence on V_g to be consistent with the idea that the high resistance states were associated with the trapping of a single charge carrier. We thus identified the mean time in the high resistance state as the trap emission time (τ_e). The mean time in the opposite state was identified as the trap capture time (τ_c).

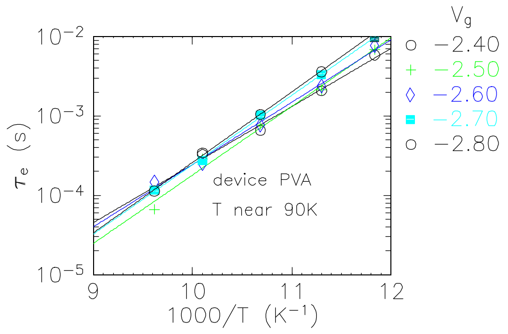

Figure 2. Semilog plot of emission time versus inverse temperature.

The duty cycles of the RTS's were found to depend primarily on V_g while the switching rates depended primarily on T, similar to the findings of others.[2,5] The corner frequency increased with T, leaving the measurement bandwidth with a change of 20-30 K.

Here we display data from one trap. Data from other traps were similar. We observed that, for fixed V_g, both τ_c and τ_e varied with T in a manner consistent with thermal activation, i. e.

$$\tau_j = \tau_{oj} \exp(E_j/kT), \qquad (1)$$

where j stands for capture or emission, E_j is the activation energy, and τ_{oj} is the attempt time. Typical capture and emission time data are illustrated in Figures 1 and 2.

Within experimental error, the activation energies for both capture and emission were independent of gate voltage. This is shown in Figure 3. For this particular RTS the activation energies were found to be $E_c \approx (115 \pm 10)$ meV and $E_e \approx (150 \pm 10)$ meV, respectively. The data of Figures 1 and 2 may be re-plotted to show how the RTS varies with gate voltage at fixed temperature. This is shown in Figure 4 for T = 90 K, confirming the strong dependence of τ_c and

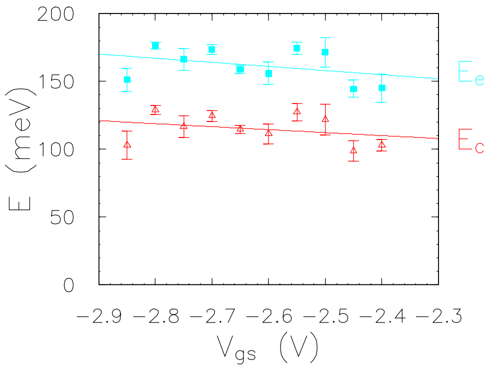

Figure 3. Variation of the activation energies for capture and emission with gate-voltage.

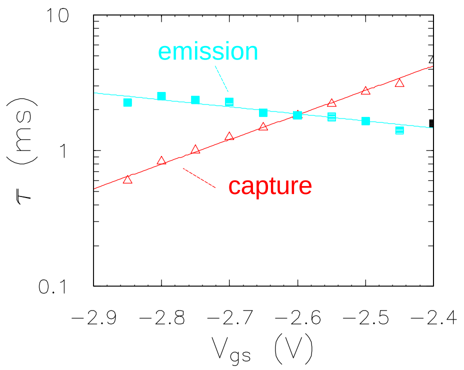

Figure 4. Gate voltage dependencies of the capture and emission times for fixed T = 90K.

weak dependence of τ_e on V_g. Referring to the above equation, this means that both prefactors may be written as

$$\tau_{j0} = \zeta_j \exp(V_g/\phi_j), \tag{2}$$

where ζ_j and ϕ_j are fit parameters independent of both T and V_g. We note, however, that there are large uncertainties in extrapolated intercepts for graphs like those in Figures 1 and 2.

The data suggest the following model. We assume that the RTS arises when a majority carrier is captured and emitted by a single trap, located 0-3 nm from the Si/SiO$_2$ interface. The empty trap level, E_t, is located below the silicon valence band edge at the interface. To be captured, a hole must first be excited to an energy E_t in the silicon valence band, then tunnel to the localized trap state in the oxide. The thermally activated behavior comes from the T-dependence of the Fermi-Dirac hole distribution. Thus, we identify the energy difference $E_c \approx E_t - E_f$ as the activation energy for capture.

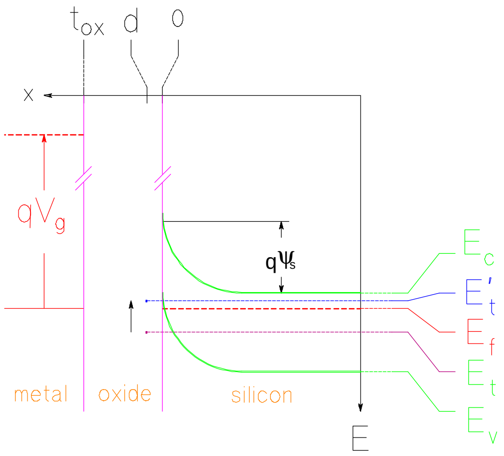

Figure 5. Band diagram showing hole trap energy levels.

Since the hole is not immediately emitted, the filled trap is assumed to undergo a lattice relaxation resulting in the lowering of the localized hole state to a new energy, E_t', with $E_t' < E_f$.[11,12,6,7] For emission to proceed, the lattice atoms must rearrange themselves, raising the trap level above E_f. This process would typically depend strongly on lattice temperature, with an activation energy $E_e = E_f - E_t'$.[11] These ideas are illustrated in Figure 5.

Several unresolved issues remain. For instance, one would expect both E_t and E_t' to vary with oxide field (i.e., gate voltage) whereas the data do not support this. Since only the capture time varies significantly with V_g we speculate that the empty trap is negatively charged while the filled trap is neutral. The V_g-dependence of τ_C might enter both through E_t and also though a V_g-dependent tunneling rate.

Very recent data for one trap shows that both capture and emission times become independent of lattice temperature below 15 K. This suggests that lattice motion other than thermal, perhaps zero-point motion or configurational tunneling, is involved in the lattice transition.

In conclusion, we have observed highly reproducible random telegraph signals in small gate-area pMOS transistors at temperatures down to 77 K. We find both capture and emission times to depend strongly on temperature (i.e., thermally activated) while only the capture time varies strongly with gate voltage. We conclude that the unoccupied trap is charged, and suggest a model involving lattice relaxation of the filled trap.

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REFERENCES

(*) This work was supported by the U. S. Department of Energy through Contract No. DE-AC04-76DP00789.

1. See, for instance, A. van der Ziel, Adv. Electron. Electron Phys. 49, 225 (1979).
2. M. J. Kirton and M. J. Uren, *Advances in Physics* **38**, 367-468 (1989).
3. John H. Scofield, T. P. Doerr, and D. M. Fleetwood, *IEEE Trans. Nucl. Sci.* **36**, 1946 (1989).
4. D.M. Fleetwood and J.H. Scofield, *Phys. Rev. Lett.* **64**, 579 (1990).
5. K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, *Phys. Rev. Lett.* **52**, 228 (1984).
6. M. Schulz and A. Papas, in *Noise in Physical Systems and 1/f Fluctuations*, ed. T. Musha, S. Sato, and M. Yamamoto (Ohmsha, Ltd, Tokyo, 1991) p. 265.
7. K. R. Farmer, in *Insulating Films on Semiconductors*, ed. W. Eccleston and M. Uren (Adam Hilger, Briston, 1991) pp. 1-18.
8. Philip Restle, *Appl. Phys. Lett.* **53**, 1862 (1988).
9. John H. Scofield and D. M. Fleetwood, *IEEE Trans. Nucl. Sci.* **38**, 1567 (1991).
10. Note that most reports of RTS's in MOSFETs have usually been associated with switching in the drain current with constant voltage bias [2].
11. L. D. Jackel, W. J. Skocpol, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, in *Proceedings of the 17th International Conference on the Physics of Semiconductors*, ed. by J. D. Chadi and W. A. Harrison (Springer-Verlag, New York, 1985), pp.221-224.
12. M. J. Kirton and M. J. Uren, *Appl. Phys. Lett.* **48,** 1270, (1986).

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[*] This work was supported by the U. S. Department of Energy through Contract No. DE-AC04-76DP00789.

[1] See, for instance, A. van der Ziel, Adv. Electron. Electron Phys. 49, 225 (1979).

[2] M. J. Kirton and M. J. Uren, *Advances in Physics* **38**, 367-468 (1989).

[3] John H. Scofield, T. P. Doerr, and D. M. Fleetwood, *IEEE Trans. Nucl. Sci.* **36**, 1946 (1989).

[4] D.M. Fleetwood and J.H. Scofield, *Phys. Rev. Lett.* **64**, 579 (1990).

[5] K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, *Phys. Rev. Lett.* **52**, 228 (1984).

[6] M. Schulz and A. Papas, in *Noise in Physical Systems and 1/f Fluctuations*, ed. T. Musha, S. Sato, and M. Yamamoto (Ohmsha, Ltd, Tokyo, 1991) p. 265.

[7] K. R. Farmer, in *Insulating Films on Semiconductors*, ed. W. Eccleston and M. Uren (Adam Hilger, Briston, 1991) pp. 1-18.

[8] Philip Restle, *Appl. Phys. Lett.* **53**, 1862 (1988).

[9] John H. Scofield and D. M. Fleetwood, *IEEE Trans. Nucl. Sci.* **38**, 1567 (1991).

[10] Note that most reports of RTS's in MOSFETs have usually been associated with switching in the drain current with constant voltage bias [2].

[11] L. D. Jackel, W. J. Skocpol, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, in *Proceedings of the 17th International Conference on the Physics of Semiconductors*, ed. by J. D. Chadi and W. A. Harrison (Springer-Verlag, New York, 1985), pp.221-224.

[12] M. J. Kirton and M. J. Uren, *Appl. Phys. Lett.* **48,** 1270, (1986).