

FABRICATION OF ENCAPSULATED INDIUM FILMS FOR MELTING EXPERIMENTS

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We describe the fabrication of submicron, multiprobe thin indium film conductors for electrical measurements above their melting transition. Problems unique to handling liquid films were overcome by using tri-level $\text{Si}_3\text{N}_4/\text{In}/\text{W}$ structures. Tungsten (W) leads made good electrical contact to, yet did not alloy with the liquid indium (In). A silicon-nitride (Si_3N_4) encapsulating layer deposited over the In/W devices prevented the indium from forming islands when liquid. Indium wires were fabricated using e-beam lithography and liftoff. Low temperature reactive sputtering technique was used to deposit the Si_3N_4 without melting the indium. The technique could be easily adapted to use with other low melting point materials.

Introduction

Successive measurements of the resistance $r(t)$ of a small, metallic conductor do not generally yield precisely the same result, but instead fluctuate about their mean value $\langle r \rangle$. Moreover, these resistance fluctuations, $\delta r(t) \equiv r(t) - \langle r \rangle$, are frequently found to have a power spectral density $S_r(f)$ that varies inversely with frequency, i.e., "1/f noise" [1]. The relative size of the phenomenon, $\langle \delta r^2 \rangle^{1/2}$, scales inversely with the conductor volume Ω , and is on the order of 10^{-8} for a 1 mm x 10 μm x 100 nm conductor. The effect has only been observed in point contact and thin film geometries.

While the origin of 1/f noise in metals is not well understood, over the last few years evidence has emerged suggesting that these resistance fluctuations are associated with slow relaxation and/or rearrangement of defects in the metal [1]. If this is indeed the case, one would not expect to observe the phenomenon in liquid metals. The only measurements on liquids, however, performed with point contacts, found no difference between the 1/f noise of liquid and solid gallium [3]. Such two-probe measurements, however, are particularly susceptible to surface effects, and may not be characteristic of the liquid metal.

Here we describe the fabrication of liquid indium samples suitable for four-probe noise measurements. By choosing a metal (In) that melts above 100 °C we were able to process the metal as a solid, making use of standard thin film deposition and patterning technology. A tungsten layer was used to make contact to the indium since the two metals do not alloy. After the multi-probe indium conductors were fabricated an insulating layer was deposited over top of them to prevent them from forming islands upon melting.

Sample Fabrication

Figure 1 shows a plan view of the sample geometry. Samples consisted of $\text{Si}_3\text{N}_4/\text{In}/\text{W}$ tri-level structures on an oxidized silicon wafer. Large tungsten probes connected the outside of the 4 mm sq. chip to indium structures occupying the inner 400 μm sq. region. Undesirable resistance and noise associated with the In/W interface was avoided by making the interface area large. The central part of the chip was covered with a Si_3N_4 layer that

extended well out over the tungsten probes. An exaggerated cross-sectional view is shown in Figure 2. Indium conductors, 500 nm wide, were patterned in the innermost ($40\ \mu\text{m}$)² region, with larger indium probes occupying the remainder of the indium pattern. The entire indium structure was fabricated in a single indium layer using e-beam lithography.

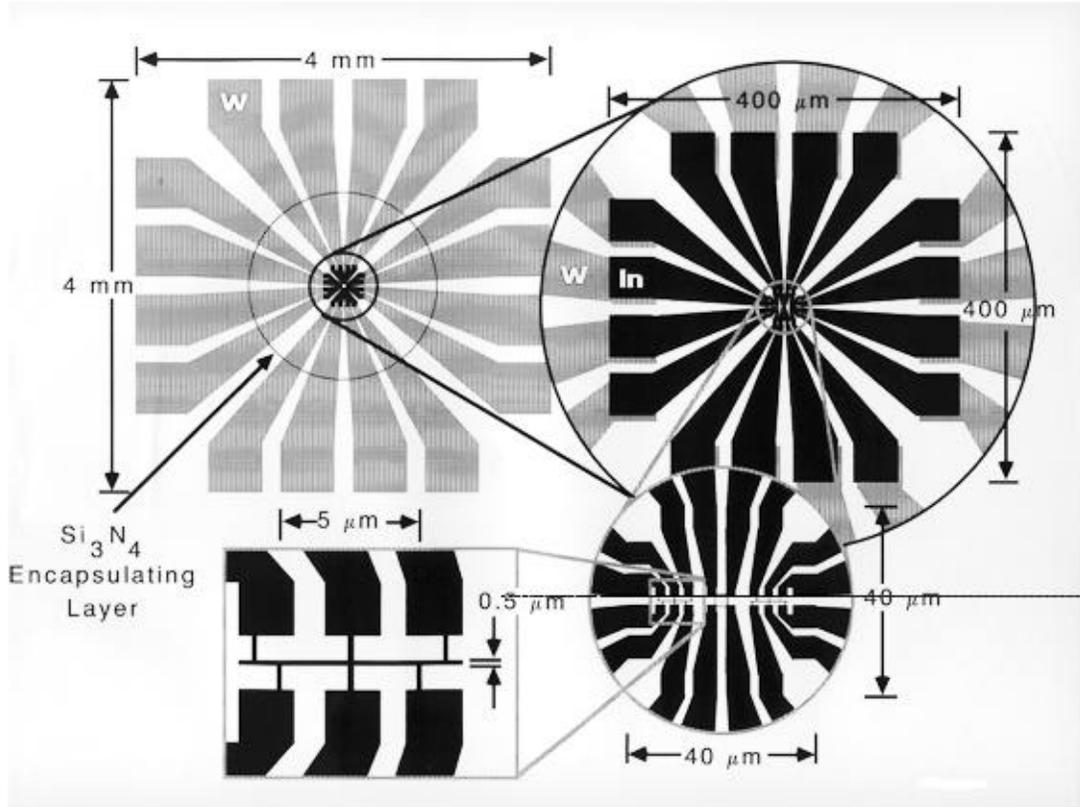


Figure 1. Plan view of sample geometry. Tungsten (W) leads make contact from outside of 4 mm sq. chip to overlapping indium (In) leads in inner $400\ \mu\text{m}$ sq. region of chip. The In leads ultimately connect to 500 nm wide indium conductors at the center of the chip. A Si_3N_4 layer is deposited over the middle of the chip to hold the liquid indium in place.

The technique is conceptually simple but its implementation required that several logistic problems be overcome: 1) fabrication of low resistance, low noise contacts, 2) fabrication of smooth (i.e., grain size $< 20\ \text{nm}$) indium films, and 3) low temperature ($T < 60\ ^\circ\text{C}$) fabrication of an encapsulating film over the indium. Below we describe the fabrication process in some detail.

The first step in the process was to prepare the tungsten base electrode. An oxidized silicon wafer¹ 2.0 in diameter, 0.020 in. thick, $<100>$ boron doped, $5\text{-}10\ \Omega\text{cm}$, was cleaned with solvents and etched in a 50:50 mixture of $\text{H}_2\text{O}_2\text{:H}_2\text{SO}_4$. A 200 nm thick layer of tungsten (nominal resistivity $30\ \mu\Omega\text{m}$) was deposited onto the wafer in a Materials Research Corp. (MRC) RF magnetron sputter system. The wafer was spin-coated with a $1.5\ \mu\text{m}$ thick layer of AZ1350J photoresist, that was subsequently UV contact exposed and developed forming lead patterns for an array of chips. The photoresist pattern was transferred to the tungsten layer by ion bombardment with 450 eV Ar^+ ions in a Commonwealth ion-mill.

¹ Silicon wafers were supplied by the Pensilco Co. with a 300-500 nm thermally grown oxide.

Milling was accomplished at an angle of 45° with stage rotation to obtain better step coverage of the indium over the tungsten. After milling, the resist was stripped by physically scrubbing in acetone using a cotton swab combined with ultrasonic agitation in boiling acetone. The process produces a 5 x 5 array of chips, each having the tungsten contact pattern shown in Figure 1. In addition to the base electrode, the tungsten pattern included alignment marks on each chip for subsequent e-beam lithography.

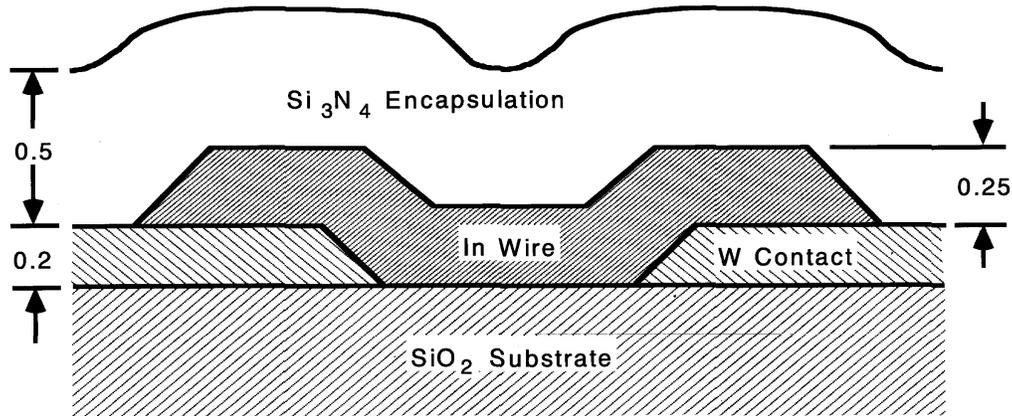


Figure 2. Cross-sectional view of the tri-level sample geometry. The horizontal axis is not drawn to scale. Film thicknesses are given in μm.

The indium liftoff stencil was fabricated using direct-write electron beam lithography in single layer resist. The wafer with the previously patterned tungsten leads and registration marks was spin-coated with a 400 nm thick layer of poly methyl methacrylate (PMMA) and baked at 160°C for one hour. The exposure was made using a JEOL JBX5DII, 50 keV e-beam lithography system. All written regions received a dose of 700 μ/cm². Since the pattern combined the high resolution multi-probe conductors with larger indium pads, the exposure was accomplished with two different beam diameters (and currents): a 60 nm beam was used to write the 40 μm sq. conductor region while a 1 μm beam was used for the 400 μm sq. probe region. The registration accuracy of the instrument was sufficient to easily allow such alignment. This technique economizes on writing time, and therefore allows wafer scale fabrication. After writing the e-beam liftoff pattern in the center of each of the 25 chips the PMMA was developed for 7 seconds in 3:7 Cellosolve (ethylene glycol mono ethylether):methanol. The wafer was subsequently subjected for 45 seconds to a 150 V oxygen plasma to remove any remaining PMMA in the exposed regions that might not have fully cleared in the developer. Following this the wafer was cleaved and indium deposition performed on a chip by chip basis.

Smooth films (i.e., small crystallites) were fabricated by evaporating indium onto chips held at 77 K. The indium was evaporated from a 1 cm diameter, resistively heated tungsten boat onto substrates held 30 cm away. Spring clips held the substrates to a liquid nitrogen cooled copper plate with a thin, uniform layer of Apiezon N-grease used to improve heat transfer. The evaporation chamber was evacuated by a 4 in. diffusion pump with a liquid nitrogen cold trap to a base pressure of 1.0 x 10⁻⁷ Torr, after which, a Meissner trap surrounding the sample, and subsequently the sample stage were cooled to 77 K. Next, substrates were "cleaned" for 10-20 min. by exposure to a 60 Hz oxygen glow discharge. Indium deposition proceeded in two stages, formation of a thin (5 nm) indium-oxide adhesion

layer, followed by a thicker (100-250 nm) indium film [4]. The thin indium layer, deposited at a rate of 0.1-0.2 nm/s, was oxidized during a 60 sec exposure to the oxygen glow discharge. The remaining indium was deposited at a rate of 3-5 nm/s. Lift-off of the unwanted indium was accomplished by gentle agitation in boiling acetone. Figure 3 is an scanning electron micrograph of an indium conductor fabricated using this technique. All samples had widths $w = (600 \pm 100)$ nm and a separation L between the outer set of voltage probes of (5.0 ± 0.2) μm . Indium thickness t ranged between 100 nm and 250 nm.

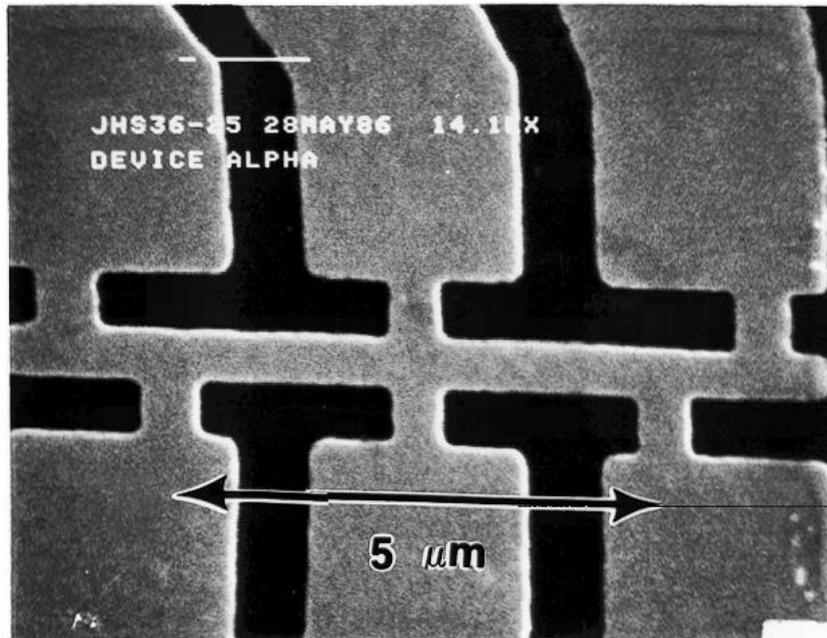


Figure 3. Scanning electron micrograph of an unencapsulated, 100 nm thick indium conductor. The conductor width $w = (600 \pm 100)$ nm and the separation between the outer voltage probes $L = (5.0 \pm 0.2)$ μm . The absence of film topology suggests a film grain size ≤ 20 nm.

Silicon-nitride (Si_3N_4) was reactively sputtered from a 6-in. silicon target in the aforementioned MRC system [5]. The circle pattern was formed by depositing through an AZ1350J photoresist liftoff pattern. (The usual 90°C prebake was not used to avoid heating the sample.) Substrate temperature was kept low during deposition by greasing the substrate to a water cooled stage. Ungreased samples melted during Si_3N_4 deposition. Nitrogen flow was maintained at 100 sccm and the gate valve throttled to yield a 10 mTorr chamber pressure. The substrate to target distance was 6.5 cm. The best results were obtained when the Si_3N_4 was deposited for 25 minutes with an RF power of 600 W, resulting in a target voltage of 340 V. The Si_3N_4 thickness was determined with an Alpha-Step surface profiler to be 500 nm.

Results

Samples fabricated in the above manner were mounted on ceramic 24-pin, dual inline packages and connection between the package and tungsten contact leads made with ultrasonically bonded aluminum wires. The temperature dependence of the indium conductor resistance near the melting transition is plotted in Figure 4. The heating curve (solid symbols) and cooling curve (open symbols) exhibited hysteresis near the melting transition. Upon

heating, the resistance of the solid indium increased linearly with temperature (T) due to phonon scattering. As T approached $T_m = (156 \pm 1)^\circ\text{C}$ from below, $r(T)$ showed noticeable deviation from linearity, then nearly doubled as the indium melted. The resistance of the liquid continued to increase with T , but at a slower rate than it had in the solid. Upon cooling, the resistance of the liquid retraced the heating curve down to T_m . The liquid, however, supercooled and solidified at $T_s = (152 \pm 1)^\circ\text{C}$.

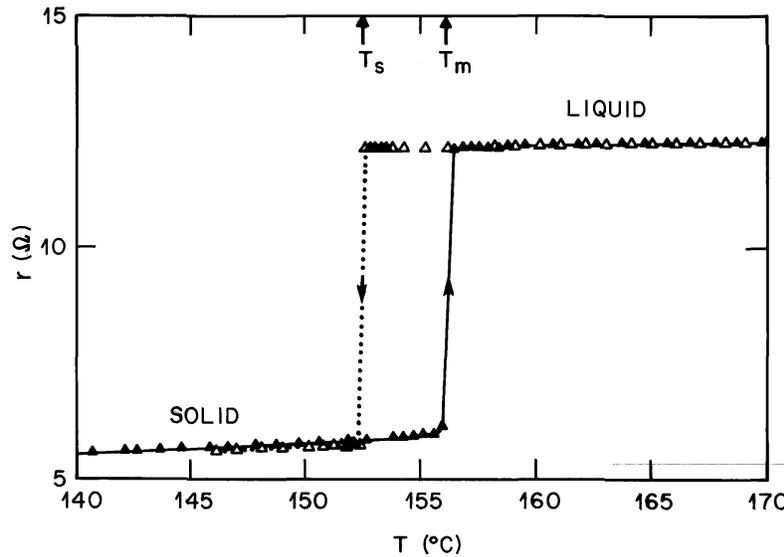


Figure 4. Temperature dependence of the resistance through the solid/liquid phase transition. The solid triangles were measured upon heating while the open triangles were measured upon cooling. The solid and dashed curves are guides to the eye. Absolute temperature is uncertain to $\pm 1^\circ$ while relative temperature is determined by interpolating time-temperature data. The melting temperature T_m and solidification temperature T_s are interpolated between the high and low resistance values.

The Si_3N_4 layer succeeded at keeping small indium structures in place, but did not have sufficient strength to hold back the 3% volume expansion upon melting of the large indium probes. The effect is more pronounced with thinner Si_3N_4 layer encapsulating and indium layers. Figure 5 shows optical micrographs of a 100 nm thick indium sample with a 150 nm Si_3N_4 layer after the indium has melted and resolidified. The higher mag. photo shows that indium structures smaller than $8\ \mu\text{m}$ have not formed islands. In contrast, the lower mag. photo clearly shows that the wider probe regions have not been rigidly held in place. This partial balling up of the large indium probes accounts for the broad melting transition of Figure 4. The effect may be reduced by using a thicker Si_3N_4 layer or by replacing the wide probes with many narrower conductors in parallel.

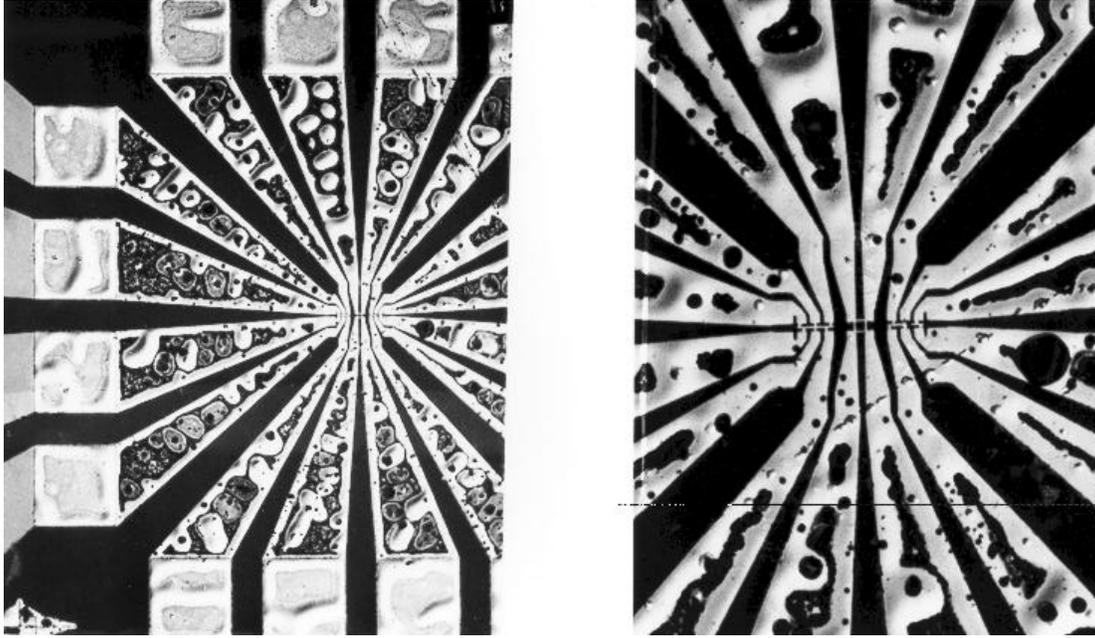


Figure 5. Optical micrograph of a 100 nm indium sample after melting. The sample is covered with a 300 nm thick Si_3N_4 layer. The horizontal line above each photo represents 100 μm . Left: 400 μm field showing partial "balling up" of the wide indium probes. Right: Magnified view showing that smaller (<8 μm) indium structures have not formed islands. Note that the right-hand, six-probe conductor was burned out during electrical measurements.

Conclusion

In summary, we have described (and demonstrated in use) a process for fabricating thin indium film conductors for transport measurements above the melting transition. The key elements were the use tungsten contacts that did not alloy with the liquid indium and encapsulation of the conductors in a strong layer of Si_3N_4 . Fabrication of submicron conductor geometries was accomplished with single level e-beam lithography and required that the indium films have a small grains size. The method could be used to fabricate structures of other materials. The strength and non-reactivity of the Si_3N_4 layer places an upper limit on the melting temperature for which the technique might be useful. The method of patterning the film in the solid state places a lower limit on the melting temperature of about 100°C.

References

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