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CORRELATION BETWEEN PREIRRADIATION 1/F NOISE AND POSTIRRADIATION OXIDE-TRAPPED CHARGE IN MOS TRANSISTORS*

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Abstract

We have performed a detailed comparison of the preirradiation 1/f noise and the radiation-induced threshold voltage shifts due to oxide-trapped and interface-trapped charge, ΔV_{ot} and ΔV_{it}, for enhancement-mode, 3-μm gate, n-channel MOS transistors taken from seven different wafers processed in the same lot. These wafers were prepared with gate oxides of widely varying radiation hardness. We show that the *preirradiation* 1/f noise levels of these devices correlate strongly with the *postirradiation* ΔV_{ot}, but not with the *postirradiation* ΔV_{it}. These results suggest that 1/f noise measurements may prove useful in characterizing and predicting the radiation response of MOS devices.

Introduction

In an ionizing radiation environment, MOS performance degrades primarily because of oxide-trapped and interface-trapped charge [1,2]. Without performing an irradiation or an equivalent *destructive* test, one cannot determine the intrinsic radiation hardness of MOS devices. The fact that a nondestructive test of MOS radiation hardness does not exist has contributed to the great practical and economical difficulties that are often associated with total-dose hardness assurance tests [3, 4].

During the past 25 years, it has been demonstrated that the low-frequency current noise ("flicker noise" or "1/f noise") of semiconductors [5-14] and metals [15-19] can be very sensitive to defects. For example, in an MOS transistor, the random capture and emission of charge carriers by traps at or near the Si/SiO_2 interface can lead to fluctuations in the number of charge carriers in the device channel, and in the channel mobility, and thus to current noise. There is much evidence that the dominant current noise of MOS transistors is associated with defects that are very similar to those responsible for radiation-induced oxide-trapped or interface-trapped charge in MOS structures [5-14].

Because similar defects are thought to be involved in both processes, we have looked for a possible correlation between the *preirradiation* current noise of MOS transistors and their radiation hardness. We find strong correlation between the *preirradiation* noise and *postirradiation* oxide-trapped charge density. In contrast, no clear correlation is observed between the *preirradiation* noise and the *postirradiation* interface-trapped charge density. The scaling of the noise with frequency, gate and drain voltage, and oxide-trapped charge density is consistent with a simple model that attributes the noise to tunneling events between the device channel and traps in the oxide. The model is considered to be quite preliminary, however, in that many questions remain unanswered regarding the exact nature of traps that cause the noise and their relationship to the postirradiation hole traps. Implications for total-dose hardness assurance testing are discussed.

Experimental Details

Samples

Noise and radiation hardness measurements were performed on chips from seven wafers. These wafers were processed in the same lot (G1916A), but received different oxidation treatments and post-oxidation anneals to vary their radiation hardness [20,21]. Noise measurements were performed on several (2-4) chips from each wafer. Several other chips from each wafer were used in performing radiation hardness measurements. Table 1 summarizes the gate-oxide growth conditions, post-oxidation annealing conditions, and oxide thickness for each of the seven wafers. Also shown for later reference are the preirradiation threshold voltage V_T, threshold shifts due to oxide-trapped and interface-trapped charge

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ΔV_{ot} and ΔV_{it} following irradiation to 100 krad(SiO_2) at a dose rate of 1 Mrad/hr, and the preirradiation 1/f-noise level K (to be discussed). All measurements of noise and radiation hardness reported here are for 3 μm x 16 μm n-channel transistors. The chips were mounted in 24-pin ceramic DIP packages.

Wafer No.	oxidation conditions	annealing conditions	t_{ox} (nm)	V_T (V)	ΔV_{ot} (V)	ΔV_{it} (V)	K ($10^{-11}V^2$)
9	15 m, 1000°C, dry	30 m, 1100°C, N_2(g)	32	0.80	-1.69	0.24	70 ± 10
10	15 m, 1000°C, dry	30 m, 1100°C, N_2(g)	32	0.90	-1.88	0.31	53 ± 11
21	25 m, 850°C, wet	none	32	0.60	-0.20	0.12	7 ± 2
22	25 m, 850°C, wet	none	32	0.65	-0.19	0.15	7 ± 2
32	30 m, 1000°C, dry	none	48	1.00	-0.52	0.32	18 ± 3
33	30 m, 1000°C, dry	30 m, 1000°C, N_2(g)	48	1.20	-3.53	0.56	130 ± 25
44	50 m, 850°C, wet	none	60	1.35	-0.76	0.56	22 ± 8

Table 1. Wafer number, oxidation and annealing conditions, oxide thickness (t_{ox}), preirradiation threshold voltage (V_T), threshold shifts due to oxide-trapped and interface-trapped charge ΔV_{ot} and ΔV_{it} following irradiation to 100 krad(SiO_2)at a dose rate of 1 Mrad/hr, and noise level (K) for each of the seven wafers.

Noise Measurements

Noise measurements were performed under constant-current bias conditions. Devices were operated in their linear regimes with both the substrate and source at ground. The noise-measuring circuit is shown in Figure 1. The drain current, I_d, was derived from a constant voltage source V_A in series with a large ballast resistor R_B (typically 100 kΩ). A second, constant-voltage source V_B was connected directly to the gate, ($V_B = V_g$). The two voltages V_A and V_B were supplied by a Hewlett Packard (HP) model 4140B constant voltage source/picoammeter.

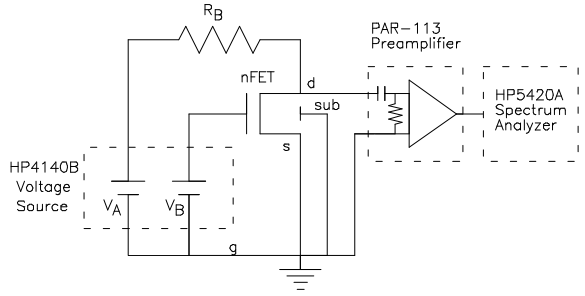

FIG. 1. Schematic diagram of the noise measurement circuit.

Fluctuations in the drain voltage were observed by first amplifying them with a Princeton Applied Research (PAR) model 113 low-noise preamplifier with a voltage gain ranging from 10^3 to 10^4. The preamplifier input was AC coupled to the drain of the sample in order to block the average drain voltage (i.e., the dc-offset $\bar{V}_d$), and the preamplifier's low-and high-pass filters were set to pass frequencies from 0.3 Hz to 30 kHz. The preamplifier output was connected to an oscilloscope for observing the voltage noise as a function of time, or to the input of an HP-5420A FFT spectrum analyzer for calculating the power spectrum of the voltage fluctuations. Both the HP-5420A spectrum analyzer and HP-4140B voltage source were controlled with a personal computer using the IEEE-488 general purpose instrument bus (GPIB). The rms-noise voltage at the output of the preamplifier typically ranged from 20-500 mV in the measurement bandwidth. Most spectra were measured for frequencies 1-255 Hz; a few measurements extended to 1.6 kHz. Power spectra for successive time records were averaged, yielding good precision after 5-10 minutes of data logging. No heroic shielding efforts were required. The noise data presented here have been corrected for amplifier gain so that they refer to fluctuations (δV_d) in the drain voltage.

Radiation Hardness Measurements

The radiation hardness of these devices was determined from measurements on chips processed identically to those used for noise measurements. Chips were irradiated in a Co-60 gamma cell (dose rate = 1 Mrad/hr) to a dose of 100 krad(SiO_2) at an oxide electric field of 3 MV/cm. I-V measurements were performed at room temperature to determine threshold voltage shifts due to oxide-trapped charge ΔV_{ot} and interface-trapped charge ΔV_{it} with the method of Winokur and McWhorter [22]. The choices of dose, dose rate, and electric field did not significantly affect the correlations shown below.

Results

Radiation Hardness

Radiation hardness results are summarized in Table 1. Values of ΔV_{ot} and ΔV_{it} are uncertain by the larger of ±30 mV and ±5%. As expected, devices with thinner oxides showed relatively smaller ΔV_{ot} and ΔV_{it} than devices with thicker oxides (e.g., compare wafers 22, 32, and 44) [23,24], and devices without high-temperature anneals showed less ΔV_{ot} than devices with high-temperature anneals [21,23,25]. Note that the differences in ΔV_{it} with these process changes are smaller and less systematic than the differences in ΔV_{ot} [21].

Noise

Log-log plots of typical measured drain-voltage noise spectra S_{Vd} versus frequency are shown in Figure 2. The lower trace was measured with zero bias current (i.e., $\bar{V}_d = 0$) while the upper trace was measured for an average drain voltage of 100 mV. The zero-bias noise, or background noise spectrum, is mainly due to three effects: 1) random thermal motion of the charge carriers in the channel (Johnson or Nyquist noise), 2) noise of the preamplifier, and 3) pick-up from the 60 Hz power lines. The frequency-independent thermal noise ($S_{Vd} = 4k_BTR_{ch}$) dominates at high frequencies while the preamplifier's 1/f-noise dominates at low frequencies. The line-frequency pick-up results in sharp spikes at 60 Hz and its (mainly odd) harmonics. This background noise is always present, and must be subtracted from measurements for non-zero bias current to determine the level of the current noise. The spikes due to 60 Hz pickup are simply ignored in the resulting analysis. The small effect of the finite ballast resistor on the measured noise was accounted for [26].

With a non-zero bias current, S_{Vd} exceeds the background noise by an amount that increases with the drain current, and is nearly inversely proportional to frequency (see the upper curve of Figure 2). This 1/f-noise, as it is called, has been observed in a variety of conductors and electronic devices [8,15,19]. The current noise, or excess noise spectrum $S_V(f)$, is defined to be the noise spectrum measured with non-zero bias current minus the background noise spectrum, $S_V(f, I_d) \equiv S_{V_d}(f, I_d) - S_{V_d}(f, 0)$. This frequency dependence was observed for all of the devices investigated. The upper trace of Figure 2 has a slope of -0.87, not the −1 of "true" 1/f-noise. This falls well within the category of what is called "generic" 1/f-noise, i.e., $S_V \propto f^{-\gamma}$ with $\gamma \approx 1$. All of the noise spectra here had slopes between -0.85 and -1.00. Similar, small deviations from a slope of −1 are commonly observed [15,19] and are not important for this study.

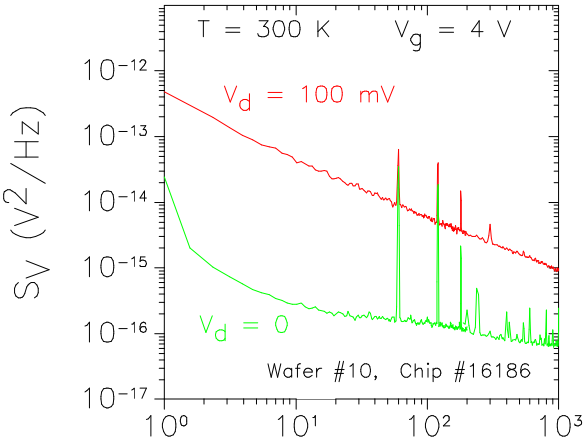

FIG. 2. Log-log plot of the observed drain voltage noise spectrum S_{Vd} as a function of frequency. The upper curve is measured with $\bar{V}_d$ = 100 mV and the lower curve with $\bar{V}_d$ = 0. The spikes in the spectra are caused by 60 Hz pickup, and are ignored in the analysis.

The excess noise spectrum S_V is a function of a number of variables: frequency f; gate-voltage, V_g; bias current, or the equivalent, average drain voltage, $\bar{V}_d$; and temperature, T. Here we report on measurements of the excess noise of n-channel MOSFETs. All measurements reported here were performed at room temperature with the devices operated in their linear regimes.

The dependence of the noise on drain-voltage is shown in Figure 3 where excess noise spectra S_V are plotted versus frequency at fixed gate-voltage for several values of $\bar{V}_d$. Each noise spectrum may be represented by $S_V = A/f^{\gamma}$, where $\gamma \approx 1$. The magnitude, A, of the excess noise spectrum varies with $\bar{V}_d$ as $A \propto \bar{V}_d^2$. This simple dependence is expected for the excess noise due to fluctuations in the channel resistance R_{ch}, since, for constant current, $\delta V_d \approx I_d \delta R_{ch} \approx \left(\overline{V_d} / \overline{R_{ch}}\right)\delta R_{ch}$ and $S_V \propto = \overline{(\delta V_d)^2}$. This $\bar{V}_d$-dependence was observed for all devices.

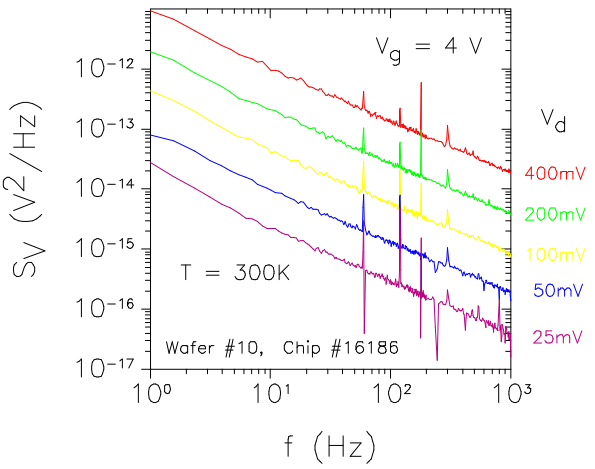

FIG. 3. Log-log plot of the excess drain-voltage noise spectrum S_V versus frequency for fixed V_g = 4 V and several average values of V_d. The spikes in the spectra are caused by 60 Hz pickup, and are ignored in the analysis.

Next we investigate the dependence of the excess noise on gate voltage for fixed $\overline{V}_d$. As the gate voltage was varied, the dependencies of S_V on f and $\overline{V}_d$ remained as described above as long as we restricted our measurements to the linear regime. The noise was found to be largest close to threshold, and decreased steadily for increasing gate voltage. Figure 4 is a log-log plot of S_V versus V_g - V_T, for fixed $\overline{V_d}$ = 100 mV and f = 10 Hz. The gate voltage dependence of Figure 4 may be expressed as $S_V \propto \left(V_g - V_T\right)^{-2}$, where V_T is the turn-on, or threshold voltage. This dependence was observed for all of the n-channel devices and is similar to that reported by others [9].

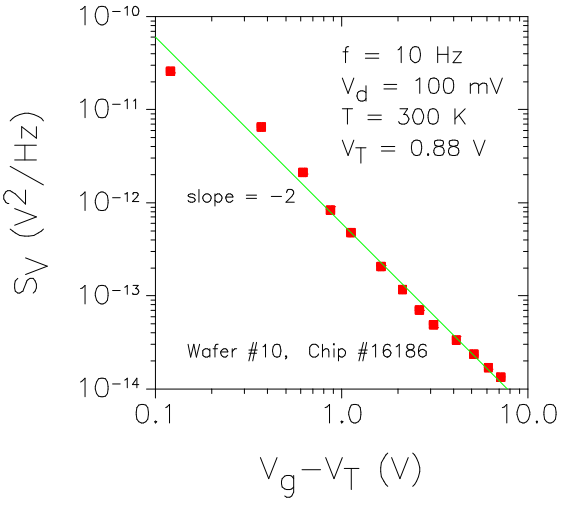

FIG. 4. Log-log plot of the excess drain-voltage noise spectrum S_V versus V_g–V_T at fixed frequency (10 Hz) and drain voltage (100 mV). The data are roughly consistent with $S_V \propto (V_g\text{-}V_T)^{-2}$, represented by the solid line which has a slope of –2.

The dependencies of the current noise of the n-channel devices on frequency, drain-voltage, and gate-voltage presented above may be simply summarized by

$$S_V(f, \overline{V_d}, V_g) = \frac{K}{f^{\gamma}} \frac{\overline{V_d}^2}{\left(V_g - V_T\right)^2}, \qquad (1)$$

where K is the "noise level" of a device. For $\gamma = 1$, K has units of V^2, and corresponds to the room temperature value of $f S_V$ at any frequency for $\overline{V}_d$ = 1 V and V_g–V_T = 1 V .

For the comparisons shown below, noise measurements were performed on 26, 3 μm n-channel devices from seven different wafers. Data were collected under computer control for a variety of frequencies, drain biases, and gate voltages. The data were used to extract the noise level K for each device. Noise levels of devices from the same wafer were found to differ by less than ±20%. Average noise levels and their uncertainties are summarized in Table 1 for each of the seven wafers. Also listed in Table 1 are the threshold voltages, determined from plots of $I_d^{1/2}$ versus V_g in saturation (i.e., $|V_d|$ = 6 V)).

Correlation Between Radiation Hardness and 1/f Noise

The data in Table 1 show no apparent correlation between the preirradiation noise levels K and postirradiation ΔV_{it}. For example, wafers 33 and 44 have the same ΔV_{it} while their noise levels differ significantly. There is, however, a striking correlation between K and ΔV_{ot}, illustrated graphically in Figure 5. The solid symbols are a log-log plot of K versus ΔV_{ot} for n-channel devices.

The noisiest devices clearly exhibit the greatest shift ΔV_{ot}, and the quietest devices exhibit the smallest shifts. Moreover, K and ΔV_{ot} appear to be linearly related. The solid line in Figure 5 is of the form $K \propto \Delta V_{ot}$ and was obtained from the data using the (unweighted) method of least squares. Therefore, for these devices, the *preirradiation* 1/f noise level may be used to predict the *postirradiation* values of ΔV_{ot}. Similar results have been observed for p-channel devices [27].

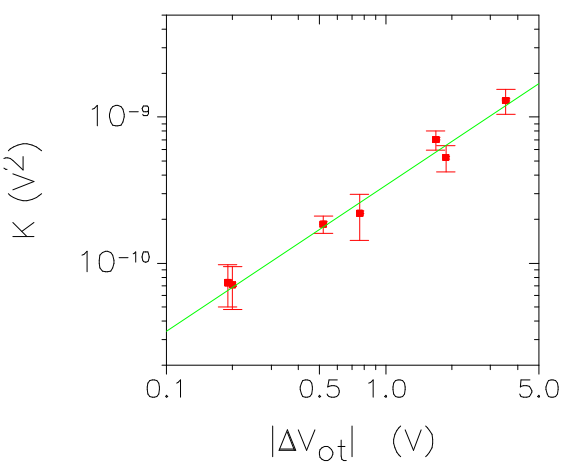

FIG. 5. Log-log plot of the noise level K versus $|\Delta V_{ot}|$. The solid line is a fit to the data of the form ($K \propto |\Delta V_{ot}|$).

Theory

Simple Trapping Model for 1/f Noise

A variety of models have been proposed to explain the 1/f noise of MOS transistors [6,8,9,11,28-30]. Here, we consider only a simple trapping model developed by Christensson, Lundstrom, and Svensson (CLS) [6,9] in which traps are assumed to exist in the oxide, uniformly distributed in energy and in space. Charge carriers tunnel in and out of these traps with a probability that decreases exponentially with distance into the oxide. The spatial distribution of traps results in a distribution of trap times, and a corresponding frequency spectrum for the excess noise [9],

$$S_V(f,\overline{V_d},V_g)=\frac{q^2}{(LwC_{ox})^2}\frac{\overline{V_d}^2}{f(V_g-V_T)^2}\frac{k_BTLwD_t(E_F)}{\ln(t_{\max}/t_{\min})} \qquad (2)$$

where C_{ox} is the oxide capacitance per unit area, $D_t(E_F)$ is the oxide trap density *per unit energy per unit area* at the trap quasi-Fermi level E_F, L and w are the transistor channel length and width respectively, q is the magnitude of the electronic charge, k_B is the Boltzmann constant, and t_{min} and t_{max} are the minimum and maximum tunneling times respectively. The above spectrum is understood to be valid for frequencies, ($1/t_{max} < f < 1/t_{min}$). Comparing Eqs. (1) and (2) we see that the model correctly describes the observed dependencies of the excess noise on *f*, $\overline{V}_d$, and V_g for our n-channel devices. It is important to note that at a given temperature, only a small fraction of the total number of oxide traps, those whose energies are within k_BT of the quasi-Fermi level, contribute to the measured 1/f noise.

Relating Noise to ΔV_{ot}

In an attempt to understand the observed correlation between ΔV_{ot} and the noise level K, we will assume that both the radiation-induced threshold shift ΔV_{ot} and the 1/f noise are related to a single oxide-trap density $D_{ot}(E) = D_t(E)$. Oxide-fixed charge is assumed not to play a role in the noise process. The model is quite preliminary, and as will be discussed below, serious questions remain unanswered regarding its precise interpretation. Nevertheless, we believe it is useful to consider the model in its present form, as it illustrates the kinds of mechanisms that can lead to the observed linear scaling of K with ΔV_{ot}.

The threshold shift ΔV_{ot} and the number per unit area of radiation-induced, oxide-trapped charges ΔN_{ot} are simply related by

$$|\Delta V_{ot}| = \frac{q\Delta N_{ot}}{C_{ox}}. \qquad (3)$$

ΔN_{ot} is presumably proportional to the total number of oxide traps N_{ot}, i.e.,

$$\Delta N_{ot} = \lambda N_{ot} = \int_{E_v}^{E_c} D_{ot}(E)dE. \qquad (4)$$

where E_V and E_C are the valence band and conduction band energies of the oxide. The proportionality constant $0 < \lambda < 1$ increases with the radiation total dose. If, as for the CLS model, the oxide traps are assumed to be uniformly distributed in energy, we then have

$$\Delta N_{ot} \approx \lambda E_g D_{ot}. \qquad (5)$$

where $E_g \equiv E_C - E_V$ is the bandgap of the oxide and D_{ot} is the (constant) oxide trap density.

Substituting Eqs. (3) and (5) into Eq. (2) and writing $C_{ox} = \varepsilon_{ox}/t_{ox}$, where t_{ox} is the thickness and ε_{ox} is the dielectric constant of the gate oxide, we find

$$S_V \approx \frac{qk_BTt_{ox}|\Delta V_{ot}|}{\lambda\varepsilon_{ox}E_gLw\ln(t_{\max}/t_{\min})}\frac{\overline{V_d}^2}{f(V_g-V_T)^2} \qquad (6)$$

Comparing Eqs. (6) and (1) we see that the above assumptions lead to the conclusion that the noise level K and oxide-trap threshold shift ΔV_{ot} are related by

$$K \approx \frac{qt_{ox}k_BT}{\lambda\varepsilon_{ox}E_gLw\ln(t_{\max}/t_{\min})}|\Delta V_{ot}|. \qquad (7)$$

For fixed oxide thickness Eq. (7) predicts the trend shown in Figure 5. For different oxide thicknesses (appropriate for our data), Eq. (7) predicts that (K/t_{ox}

$\propto |\Delta V_{ot}|$). Figure 6 is a log-log plot of K/t_{ox} versus $|\Delta V_{ot}|$. The graph suggests strong correlation between these two variables, and is clearly consistent with the model prediction, illustrated by the solid line in Figure 6. Reasonable estimates of the various quantities in Equation (7), however, give noise levels an order of magnitude higher than those observed.

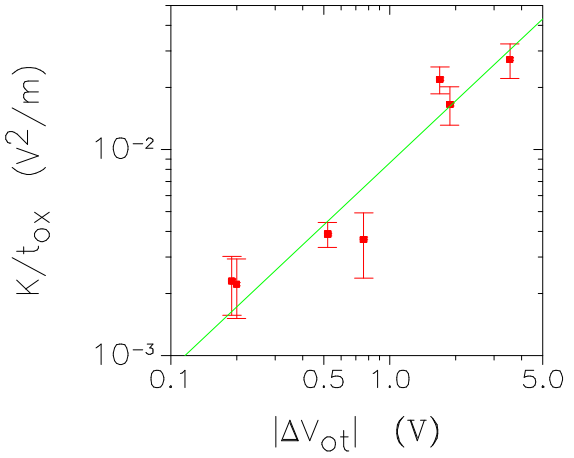

FIG. 6. Log-log plot of the noise level K/t_{ox} versus $|\Delta V_{ot}|$. The solid line is a fit to the data of the form $K/t_{ox} \propto |\Delta V_{ot}|$.

For instance, if we assume that $t_{max}/t_{min} \approx 10^{12}$, and take T = 300 K, L = 3 μm, w = 16 μm, E_g = 9 eV, $\varepsilon_{ox}/\varepsilon_o = 3.9$ (ε_o being the permittivity of free space), $\lambda = 0.1$ (appropriate for a total dose of 100 krad(SiO_2)), and combine these with the oxide thickness and measured ΔV_{ot} for Wafer No. 33 (see Table 1), the above equation gives a noise level $K \approx 150 \times 0^{-11}$ V^2 compared to the measured value of 130×10^{-11} V^2. Therefore, while the model correctly predicts a linear relationship between K and ΔV_{ot}, in its present form, it does not give the observed noise magnitude.

Discussion

In addition, and possibly related to, its over estimation of the magnitude of the 1/f noise, the above model has several other flaws as well. For one thing, the defects that give rise to ΔV_{ot} are known to trap holes through irradiation, and not electrons [1]. Therefore, these traps may not be expected to generate noise in n-channel devices where the majority carriers are electrons. Prior to irradiation, though, a precursor defect to the radiation-induced hole trap may be present [1], the number of which is proportional, but not equal, to the measured ΔN_{ot}. These precursor defects might, in fact, trap both holes and electrons. Hole traps and electron traps are known to exist in SiO_2 [31,32]. Oxygen vacancies can, in some cases, trap both holes and electrons [33]. So it may be very natural that the noise of n-channel devices scales with the number of oxide traps, though more work is required to understand the detailed nature of the interaction.

Another shortcoming of the above model is that it does not consider the effects of charge trapping on channel mobility, which may in fact, be more important than the effects of trapping on the number of majority carriers [29]. Several authors have attempted to incorporate both number and mobility fluctuations into a trapping model for 1/f noise [9,29]. Accounting for these effects is not likely to dramatically alter the noise magnitude, but it may alter the dependence on gate voltage [29], and may also give hole trapping a mechanism for generating noise in an n-channel device.

Comparison with Previous Work

We are not the first to report a correlation between 1/f noise and oxide *traps* in MOS transistors [9,11,12]. Correlations between 1/f noise levels and *interface trap* densities have also been reported [5,7,13,14,34]. Tunneling models, similar to the model presented above, are now widely believed to explain the noise of MOSFETs. Such models implicitly attribute the noise to *oxide traps* (e.g., oxygen vacancies) near, but not at, the *Si/SiO*$_2$interface. It is difficult to understand how *interface states* (e.g., dangling silicon bonds) with their fast relaxation, can cause the observed low frequency noise below, say 10 Hz [30]. Correlations between noise and interface traps might be explained in terms of a two step trapping model, involving both the fast interface states and the slower oxide states [11].

It is, of course, possible that some unspecified defects cause the noise, and correlations between 1/f noise and interface traps and/or oxide traps merely reflect a tendency for a variety of defects to be present in proportional numbers, at or near the *Si/SiO*$_2$ interface. Whether or not it is explicitly stated, such an argument must always be used to explain correlations between 1/f noise and *interface trap* or *oxide trap* densities measured using C-V or conductance measurements. Such measurements yield trap densities near midgap, while the 1/f noise is determined by traps near the quasi-Fermi level, i.e., near the appropriate band edge [10]. Therefore, traps measured with C-V or conductance measurements are never the same ones that cause the noise. Instead, one must assume that analogous traps are present in similar numbers at other energies.

The absence of correlation between K and ΔV_{it} may indicate that the 1/f noise is more sensitive to

oxide- than to interface-traps. In future studies, it would be interesting to see whether *postirradiation* 1/f noise still scales with ΔV_{ot}, or whether ΔV_{it} also begins to contribute significantly to the 1/f noise. We intend to extend our measurements to include a wider range of f, V_g, and T. Temperature-dependent measurements will be crucial for determining the energy dependence of traps that cause the noise [10,15].

Implications for Hardness Assurance Testing

The strong correlation between the preirradiation 1/f noise and the postirradiation oxide-trapped charge demonstrated in Figures 5 and 6 suggests that, whatever its precise origin, measurements of 1/f noise may be very useful in radiation testing. For example, if similar correlations between the preirradiation 1/f noise magnitudes and radiation-induced defects are found in other devices, it may be possible to define 100%, nondestructive screens for hardness assurance testing of discrete MOS transistors, and for simple circuits in which individual transistors can be isolated. While the results shown here are very promising, additional work is needed to demonstrate that such screens can be successfully developed and applied in a practical hardness assurance program. It may also be very difficult to apply 1/f noise measurements as a nondestructive screen of the radiation hardness of more complex integrated circuits. Whatever the outcome of any future efforts to apply 1/f noise in a hardness assurance program, the results of Figures 5 and 6, as well as much other work in the literature [5,7,9-14], clearly show that 1/f noise measurements can provide a sensitive probe of defects at or near the Si/SiO_2 interface. Thus, 1/f noise measurements should prove very useful in characterizing the radiation response of MOS devices.

Conclusions

We have found a strong correlation between the *preirradiation* 1/f noise levels of transistors and the density of radiation induced oxide-trapped charge. In contrast, the *preirradiation* 1/f noise does not correlate with the *postirradiation* density of interface traps. Measurements at other temperatures and frequencies will yield more information about the oxide trap distribution relevant to the radiation hardness of the device, and should provide additional insight into the origin of 1/f noise in MOS devices and its link to radiation hardness. The strong correlation between the preirradiation 1/f noise and radiation-induced oxide-trapped charge demonstrates that 1/f noise measurements can be very useful in characterizing the radiation response of MOS devices, and suggests that it may be possible to define nondestructive tests of MOS transistor radiation hardness using 1/f noise measurements.

Acknowledgments

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