Proc. of the 24th IEEE Photovoltaic Specialists Conference (IEEE, New York, 1995), pp. 291-294.

ADMITTANCE MEASUREMENTS ON $Cu(In,Ga)Se_2$ POLYCRYSTALLINE THIN-FILM SOLAR CELLS

John H. Scofield
Physics Department, Oberlin College, Oberlin, OH 44074

M. Contreras, A. M. Gabor, and R. Noufi
National Renewable Energy Laboratory, 1617 Cole Blvd., Golden, CO 80401, USA
and
J. R. Sites, Physics Department, Colorado State University, Ft. Collins, CO 80523, USA

ABSTRACT

We have measured the complex admittance for approximately 30 CIS and CIGS polycrystalline thin film solar cells having efficiencies of 12% or better. Measurements were performed for frequencies ranging from 1 to 1000 kHz and bias voltages from -2.0 to 0.4 V and were usually at room temperature. Capacitance versus voltage data were used to extract effective charge densities. Frequency-dependent capacitance and conductance data revealed information about trapping. While results vary from cell to cell, several common features emerge from the data. These results are described in this paper.

INTRODUCTION

The complex admittance, $\mathbf{A}(\omega) = G(\omega)+j\omega C(\omega)$, of a reverse-biased diode contains considerable information about the junction [1]. Here $\omega = 2\pi f$ is the angular frequency and $G(\omega)$ and $C(\omega)$ are the diode conductance and capacitance respectively. The capacitance of a well-behaved reverse-biased diode, for instance, gives a direct measure of the depletion width. For an ideal, uniformly doped, one-sided junction, a plot of $1/C^2$ versus V (bias voltage) yields a straight line, the slope of which may be used to determine the lesser of N_a and N_d. For non-uniform doping, the doping density as a function of distance from the junction may be obtained from the derivative, $d(1/C^2)/dV$.

The ac capacitance measures the mobile charge density over a small distance δW (determined by the ac voltage δV) at the edge of the depletion width W (determined by the dc bias V). Trapped charge can respond to low frequencies but not to high frequencies, where high and low are determined by the trap's relaxation time. Thus, traps contribute to the low-frequency, but not the high-frequency, capacitance and, accordingly, trap distributions may be extracted from measurements of capacitance versus frequency [2]. Finally, zero-bias measurements of the conductance for various frequencies and temperatures may be used to further characterize trapping states [3, 4].

EXPERIMENTAL DETAILS

We have performed admittance measurements on twenty-nine, 9-16.4% efficient, 0.43 cm^2 area, polycrystalline, thin-film solar cells solar cells from 16 different $CuInSe_2$ (CIS) and $Cu(In,Ga)Se_2$ (CIGS) absorber layer depositions. Samples were fabricated at the National Renewable Energy Laboratory (NREL) on soda-lime glass substrates with the usual n^+-ZnO/i-ZnO/i-CdS/CIGS/Mo structure. Absorber layers were formed from precursor films evaporated from elemental sources (Cu, In, Ga, and Se), in most cases using a 3-stage coevaporation process [5]. We have also looked at cells with absorber layers fabricated using the recrystallization method [6], the in-line source process [7] and Se-vapor selenization [8]. The properties of several of these cells are summarized in Table I.

Admittance measurements were typically performed on two or more devices on the same substrate, in the dark at room temperature for frequencies ranging from 1 to 1000 kHz and bias voltages ranging from -2.0 to 0.4 V. In a few cases, measurements were performed at frequencies as low as 100 Hz and, in one case, for temperatures ranging from -20° to 75°C. Data were either logged at constant V while scanning log(f) or at constant f while scanning V. In both cases, devices were held at zero bias for a few minutes then the bias was switched to the desired value for the beginning of the scan. For bias scans, V was stepped from V_{min} to V_{max} in 25, 100 mV increments. Each scan took approximately 2 mintues.

RESULTS

The detailed results of measurements varied from substrate to substrate, but were similar for cells on the same substrate whenever the cells showed similar current-voltage (J-V) characteristics. Despite their many differences high-efficiency cells (η > 12%) shared several common features; these include: 1) a frequency independent capacitance for f > 1 kHz, 2) a voltage-dependent shunt resistance, 3) the existence of slow transient states, and 4) effective absorber carrier

densities which increase away from the junction. Below we elaborate on these four topics.

Cell ID	Absorber	J-V Measurements				Illuminated	
		η %	V_{oc} mV	J_{sc} mA/cm^2	FF %	R_s Ω cm^2	A
C217-12-5	CIS/selenize	11.0	473	36	65	0.8	1.8
M1187-23-1	CIGS/3-stage	10.0	529	28½	66	0.2	2.1
M1201-14-4	CIS/3-stage	13.2	485	36½	75	0.15	1.2
M1174-14-3	CIGS/3-stage	15.9	649	32	76½	0.25	1.55
C253-23-9	CIGS/3-stage	15.8	611	34	76	0.3	1.4
C266-23-8	CIGS/3-stage	16.4	660	31½	78½	0.1	1.3

TABLE I. Summary of cell properties including efficiency (η), open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (FF), series resistance (R_s), and ideality factor (A).

Dependence of Capacitance on Frequency

The first common feature of high-efficiency cells was a capacitance that was relatively independent of frequency. Fig. 1 shows typical C(f) curves for several different bias voltages. Only the forward-bias scan shows a noticeable increase in C as f $\rightarrow$ 0. The high-frequency turn-up in the measured capacitance is an artifact associated with a resonance due to the self-inductance of the measurement circuit [9]. When compared with cells from several years ago these cells show significantly lower concentrations of traps that respond on the 1-1000 μs time scale [2]. Of course, significant numbers of traps might be present whose relaxation times are slower than 1 ms. In fact, transient behavior, discussed below, suggests the presence of traps with slower response times.

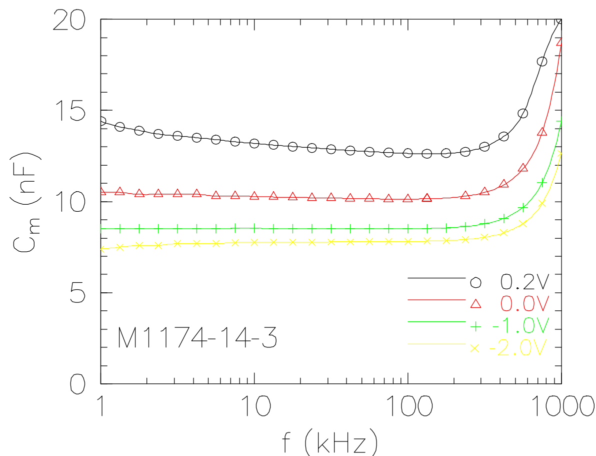

FIG. 1. Graphs of the measured capacitance versus log frequency for four different biases for a 15.9% CIGS cell. The high-frequency turn-up is associated with a resonance due to the self-inductance of the connecting cables.

Bias-Dependent Shunt Resistance

The second feature, common to most cells, was the observation of a voltage-dependent shunt resistance, $R_{sh}(V)$. To appreciate how this shows up in the admittance measurements it is useful to compare the data with the calculated admittance of a three-component circuit consisting of a small resistance (R_s) in series with a parallel combination of a capacitance (C) and a (shunt) resistance (R_{sh}). Even when R_s, R_{sh}, and C are ideal (i. e., voltage- and frequency-independent) the real part, $G_m(\omega)$, of the measured admittance is expected to vary with frequency. For the ideal case, $G_m(\omega)$ asymptotically approaches $1/R_{sh}$ as $\omega \rightarrow 0$ and $1/R_s$ as $\omega \rightarrow \infty$ [9]. Thus, we expect $G_m(\omega \rightarrow 0) = 1/R_{sh}$.

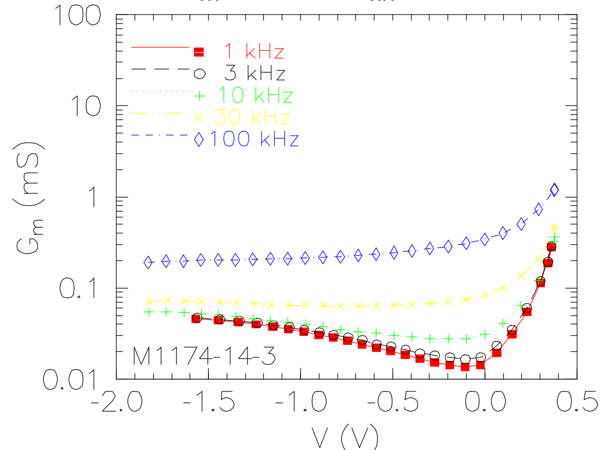

FIG. 2. Semilog graphs of the measured conductance versus bias voltage for various measurement frequencies for CIGS device M1174-14-3.

Typical voltage-scans of the measured conductance for different frequencies are graphed in Fig. 2. The higher-frequency data (e. g., f = 30 and 100 kHz) are consistent with expectations for an ideal circuit, allowing for the voltage-dependence of the depletion capacitance. At lower frequencies, however, measured conductances exhibit a voltage dependence consistent with calculations for the model circuit only if R_{sh} is assumed to change with V. For device M1174-14-3 shown, the shunt resistance has a maximum near zero bias and decreases by about a factor of 4 as V ranges from 0 to -2 V. For some cells, the shunt resistance varied by less than a factor of 2 over this range of bias. For an 11% efficient cell made by selenization, R_{sh} varied by about a factor of 30 over this range of bias (see Figure 3).

Proc. of the 24th IEEE Photovoltaic Specialists Conference (IEEE, New York, 1995), pp. 291-294.

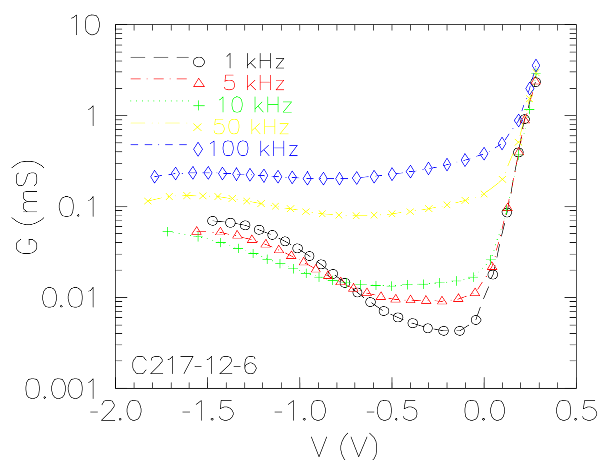

FIG. 3. Semilog graphs of the measured conductance versus bias voltage for various measurement frequencies for 11% efficient CIS device C217-12-6.

Slow Transient Response

The third common feature was the observation of transient current response, I(t), when cells were switched from zero to reverse bias, especially for V < –1 V. Prior to such a measurement, cells were typically held at zero bias for at least several minutes. When the applied voltage was rapidly switched to V_0, the magnitude of the resulting current was initially low and increased with time, asymptotically approaching some steady value. The importance of this effect became larger, the more negative V_0. For V_0 > –0.5 V, the effect was not noticeable. For V_0 < –2 V, transient effects were quite noticeable. This effect is related to the voltage-dependent shunt resistance, and may well be associated with other transient effects, such as those reported for V_{oc} [10].

Both the transient current and bias-dependent, low-frequency conductance ought to show up in J-V measurements. Most J-V measurements on these CIS and CIGS devices were been performed for -0.5 ≤ V ≤ 1.0, a range of bias in which both of these effects seem to have negligible consequences. We have performed additional J-V measurements on several devices to -2 V bias. For these measurements we have varied both the voltage sweep rate and direction. Figure 4 shows the results of such measurements for a device in which transient effects were particularly pronounced. Tabulated in the figure inset are the delay times between 10 mV changes in the bias voltage.[1] When the bias voltage was swept in the opposite direction (i.e., from 0.5 to -2.0 V) the reverse current did not show a minimum near -1.6 V, but instead, continued to increase the more negative the bias. We conclude that the zero J for -2V bias in Fig. 4 is due to the fact that the cell has not been allowed sufficient time to reach the steady-state current associated with this bias. It appears that all of these transient effects are associated with the capture and emission of carriers from very slow traps.

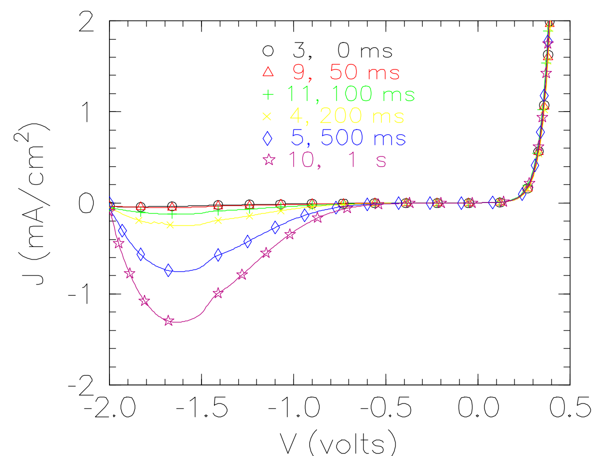

FIG. 4. J-V measurements for 11% efficient CIS device C217-12-6 for various sweep rates. Tabulated in the inset are delay times Δt, such that sweep rates were 10mV/Δt.

C-V Measurements

Room-temperature C-V measurements on all devices have been analyzed to determine the effective hole density, p(x), in the absorber as a function of distance x from the interface, assuming an abrupt, one-sided junction. The results for several cells with absorber layers fabricated using the 3-stage, indium-containing precursor method are shown in Fig. 5.

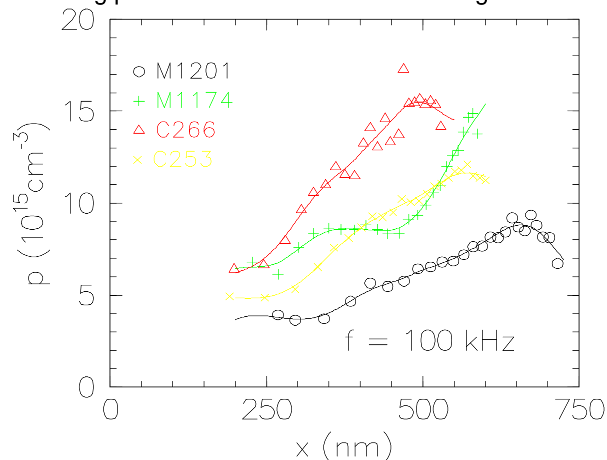

FIG. 5. Effective absorber layer carrier densities deduced from C-V measurements at 100 kHz.

Evidence for Localized Trapping State

Finally, admittance measurements from one CIGS cell show evidence of a narrow distribution of traps. Fig. 5 shows graphs of room-temperature conductance versus bias for various measurement frequencies. These curves exhibit peaks in the conductance superposed with G(V) behavior similar to that shown in Fig. 2. The peak

---

1 Prior to a measurement, the voltage was held at zero bias. A J-V measurement was subsequently performed by rapidly changing the bias voltage to -2.0 V, then increasing V in 10 mV steps, delaying a time Δt at each voltage step.

voltage, V_p, was found to vary linearly with the logarithm of the measurement frequency. Measurements, performed at temperatures between -20 °C and 75°C, are consistent with thermally-activated behavior with an activation energy of 560 meV. The results suggest the presence of a trap near the interface at an energy close to midgap.

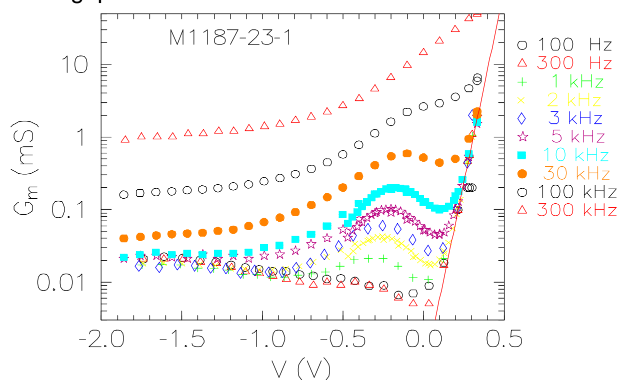

FIG. 6. Graphs of conductance versus bias V for various measurement frequencies for a CIGS device showing conductance peak indicative of a narrow distribution of traps.

DISCUSSION AND CONCLUSIONS

The first obvious conclusion is that the 14-16% efficient CIS and CIGS cells we have looked at generally have considerably fewer "fast" traps than did the 10-12% CIS cells of a few years ago, as evidenced from their frequency-dependent capacitance. This is consistent with the observation that these cells have higher conversion efficiencies and diode ideality factors closer to unity.

Second, the best CIS and CIGS cells all have effective charge densities, as determined from C-V measurements, which increase with distance from the junction. Also, more efficient CIGS cells appear to have higher carrier densities. This clearly has limits. however, as the highest carrier density was observed for a CGS cell which had very low conversion efficiency.

Third, very slow transient effects (10's of seconds to a few hours) continue to be observed, which appear to be associated with the capture and emission of carriers by traps. We suspect that these are related to time-dependent V_{oc} [10] but further work is required.

Finally, a voltage-dependent conductance has been observed for all devices in reverse bias. On the one hand this may simply be more evidence for the presence of a "2nd junction," previously reported for a variety of devices. On the other hand, it may be that careful comparison of conductance data with model calculations might shed light on critical device structures.

ACKNOWLEDGMENTS

The authors would like to thank R. Sasala, I. Eisgruber, and X. Liu for assistance with the admittance measurements and useful conversations, A. Tennant for assistance with J-V measurements, and J. Tuttle, B. Keys, and R. Ahrenkeil for helpful discussions. One of the authors (JHS) was supported, in part, by an Associated Western Universities - Department of Energy Faculty Sabbatical Fellowship. This work was performed at NREL and CSU under contract No. DE-AC36-83CH10093 to the U. S. Department of Energy.

REFERENCES

[1] See, for instance, S. M. Sze, *Physics of Semiconductor Devices, 2nd edition* (John Wiley & Sons, New York, 1981).

[2] Peter H. Mauk, Hossein Tavakolian, and James R. Sites, "Interpretation of thin-film polycrystalline solar cell capacitance," *IEEE Trans. Electron Devices* **ED-37** (2), 422-427 (1990).

[3] D. L. Losse, "Admittance spectroscopy of impurity levels in Schottky barriers," *J. Appl. Phys.* **46** (5) 2204-14 (1975).

[4] L. B. Fabick and K. L. Eskenas, "Admittance spectroscopy and application to $CuInSe_2$ photovoltaic devices," in *Proc. of the 18th IEEE PVSC,* Oct. 21-25, 1985, Las Vegas, pp. 754-757.

[5] A. M. Gabor, J. R. Tuttle, D. S. Albin, A. L. Tennant, M. A. Contreras, and R. Noufi, in *Proc. 12th NREL P. V. Program Review Meeting,* Oct. 13-15, 1993, Denver, CO (AIP, 1994).

[6] J. R. Tuttle, M. Contreras, A. Tennant, D. Albin, and R. Noufi, "High efficiency thin-film $Cu(In,Ga)Se_2$-based photovoltaic devices: progress towards a universal approach to absorber fabrication," in *Proc. 23rd IEEE PVSC,* May 10-14, 1993, Louisville, KY, pp. 415-421.

[7] M. A. Contreras, J. Tuttle, D. Albin, A. Tennant, and R. Noufi, "Validation of an in-line evaporation process for large-scale production of $CuInSe_2$-based solar cells," in *Proc. of the 23rd IEEE PVSC,* May 10-14, 1993, Louisville, KY, pp. 486-490.

[8] D. S. Albin, et al., "Progress towards higher efficiency $CuInSe_2$ and $Cu(In,Ga)Se_2$ solar cells by Se-vapor selenization," *in preparation*.

[9] J. H. Scofield, "Effects of series resistance and inductance on solar cell admittance measurements," *submitted for publication*.

[10] R. A. Sasala and J. R. Sites, "Time dependent voltage in $CuInSe_2$ and CdTe solar cells," in *Proc. of the 23rd IEEE PVSC,* May 10-14, 1993, Louisville, KY, pp. 543-548.