Reconciliation of Different Gate-Voltage Dependencies of 1/f Noise in n-MOS and p-MOS Transistors

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We have examined the 1/f noise of 3 μm x 16 μm, n- and p-MOS transistors as a function of frequency (f), gate-voltage (V_g), and temperature (T). Measurements were performed for 3 Hz ≤ f ≤ 50 kHz, 100 mV ≤ $|V_g-V_{th}|$ ≤ 4 V, and 77 K ≤ T ≤ 300 K, where V_{th} is the threshold voltage. Devices were operated in strong inversion in their linear regimes, and biased with a constant drain current (I_d). In all cases the excess drain-voltage noise spectrum, S_{V_d} scaled with $f^{-\gamma}$, where $\gamma \approx 1$, i.e., "1/f noise," and, for sufficiently low currents, $S_{V_d} \propto V_d^2$. At room temperature we find that, for n-MOS transistors, $S_{V_d} \propto V_d^2/(V_g-V_{th})^2$, and for p-MOS transistors, we generally find that $S_{V_d} \propto V_d^2/(V_g-V_{th})$, consistent with trends reported by others. At lower temperatures, however, the results can be very different. In fact, we find that the temperature dependence of the noise and the gate-voltage dependence of the noise show similar features, consistent with the idea that the noise at a given T and V_g is determined by the trap density, $D_t(E)$, at trap energies E = E(T,V_g). Both the T- and V_g-dependencies of the noise imply that $D_t(E)$ tends to be constant near the silicon conduction band edge, but increases as E approaches the valence band edge. It is evidently these differences in $D_t(E)$ that lead to differences in the gate-voltage dependence of the noise commonly observed at room temperature for n- and p-MOS transistors.

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Introduction

A variety of measurements of the excess noise of metal-oxide-semiconductor field-effect transistors (MOSFETs) suggests that their noise is associated with capture and emission of charge carriers by localized traps at, or near, the Si/SiO_2 interface [1, 2]. In very small devices, discrete fluctuations associated with the capture and/or emission of single charge carriers may be observed [1, 3], especially at cryogenic temperatures. Superposition of the noise of many fluctuators leads to the ubiquitous inverse frequency dependence commonly observed in larger area devices [1]. A 1/f noise spectrum has been shown to result from superposition of thermally activated processes with a uniform distribution of activation energies [4, 5] or from tunneling processes with a uniform distribution of tunneling distances [6]. Uniform distributions are not necessary, however, as 1/f-like noise can result from a log-normal distribution of switching times [7].

One of the simplest trapping models applied to MOSFETs assumes a distribution of traps that is both uniform in space (throughout the oxide) and in energy (throughout the SiO_2 band gap) [8]. These traps produce a fluctuating trapped charge and, correspondingly, a fluctuating "effective" gate-voltage (δV_g) whose power spectral density (S_{V_g}) may be readily calculated. If a MOSFET is operated in its linear regime with constant drain current (I_d) and gate-voltage (V_g) bias, the power spectral density (S_{V_d}) of the resulting fluctuations in the drain-voltage (V_d) has been calculated to be

$$S_{V_d}(f) = \frac{V_d^2}{(V_g - V_{th})^2} S_{V_g}(f) \approx \frac{V_d^2}{(V_g - V_{th})^2} \frac{e^2}{C_{ox}^2} \frac{k_b T D_t}{LWf \ln(t_1/t_0)}, \quad (1)$$

where f is the frequency, V_{th} is the threshold voltage, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate capacitance per unit area, t_{ox} and ε_{ox} are the oxide-thickness and -permittivity, respectively, e is the fundamental unit of charge, LW is the gate area, k_b is the Boltzmann constant, T is absolute temperature, D_t is the number of traps per unit energy per unit gate area, and τ_1 and τ_2 are minimum and maximum tunneling times associated with arbitrary maximum and minimum tunneling distances assumed for the trap distribution [8, 9].

Measurements of 1/f noise in n-MOS devices have frequently confirmed the above scaling with $V_d^2/(V_g-V_{th})^2$ [10-16]. This is considered to be strong evidence for the trapping model [10, 11]. In p-MOS devices, a more complicated dependence on gate-voltage is often observed [10-13, 15, 17], one that may often be made consistent with Eq. (1) by making the ad hoc assumption that $D_t \propto (V_g - V_{th})$ [10]. It has been suggested that the V_g-dependence may be directly related to a trap density that increases as one approaches the valence band edge [12, 17]. Still others have

cited the different gate-voltage dependence for the noise of p-MOS transistors at room temperature as evidence for the dominance of mobility fluctuations [10, 11].

To date, nearly all comparisons of the gate-voltage dependence of the 1/f noise of n- and p-MOS transistors have been performed at room temperature. In the past, significant progress in understanding the origin of 1/f noise in metals has been made by detailed studies of the temperature dependence of the noise and its relation to defect energy distributions [7, 18, 19]. It is therefore interesting to see whether studies of the temperature dependence of the 1/f noise of MOSFETs might lead to similar insight into variations of $D_t(E)$ that could provide information about the differences in gate-voltage dependence for the room temperature 1/f noise of n-MOS and p-MOS transistors. In this regard, the noise of n-MOS devices has been reported to show little variation with temperature [9, 13, 15, 20], while the noise of p-MOS transistors shows considerable temperature variation [13, 15, 21]. In one case the T-dependence of the noise of a p-MOS device has been used to infer the energy dependence of the trap density [21], but the resulting trap distribution has been questioned [22, 23].

Here, we examine both the gate-voltage and temperature dependencies of the 1/f noise of n-MOS and p-MOS transistors fabricated on the same chips. We find the room temperature gate-voltage dependence of the 1/f noise to be roughly consistent with that reported by others. For n-MOS transistors, we find that the noise varies weakly with T, consistent with the expected linear dependence in Eq. (1) assuming nearly constant $D_t(E)$, but for p-MOS transistors we find a much stronger T-dependence. Based on these results we hypothesize that the gate-voltage and the temperature dependencies of the noise of MOS transistors are related, both being derived from the energy dependence of the trap distribution, $D_t(E)$. Accordingly, we infer that for p-MOS devices the observed V_g-scaling arises from a non-uniform $D_t(E)$. This is confirmed by examining the gate-voltage dependencies of the noise of both n-MOS and p-MOS transistors at lower temperatures. For both p- and n-channel devices we find that $S_{V_d}(f) \propto V_d^2 (V_g - V_{th})^{-2}$ at temperatures where $S_{V_d}(f) \propto T$, and that the gate-voltage dependence of S_{V_d} deviates from this simple relation whenever the temperature dependence is much stronger. We conclude that the 1/f noise in the p- and n-MOS transistors we have studied can both be described with a simple trapping model.

Experimental Details

Room temperature noise and d. c. conductance measurements have been performed on 15 n-channel and 15 p-channel, enhancement-mode MOS transistors from seven wafers fabricated at Sandia National Laboratories in lot G1916A. The seven wafers were prepared identically except for the growth and annealing of their gate-oxides [2, 24]. Here we report measurements at temperatures ranging from 77-300K from both a p-MOS and an n-MOS transistor on single chips from each of two of these wafers, one designated W10 and the other W44. W10 was fabricated with a non-radiation-hardened oxide having a high density of oxide traps while W44 was fabricated with a moderately hard oxide having a much lower density of oxide traps [2, 9, 24]. While details vary, trends in the noise of other n-MOS and p-MOS devices were generally consistent with the data displayed here. Properties of the four devices are summarized in Table I. Listed are the gate lengths (L) and widths (W), donor (N_d) and acceptor (N_a) doping densities, oxide thicknesses (t_{ox}), and the room-temperature ($V_{th}(300K)$) and liquid-nitrogen ($V_{th}(77K)$) threshold voltages. All measurements were performed with devices operated in strong inversion in their linear regimes with their sources and substrates grounded. Threshold voltages were determined from measurements of the d. c. channel conductance versus gate-voltage in the linear regime.

TABLE I. Device parameters for the four transistors used in this study. LW is the gate area, N_d and N_a are the donor and acceptor densities, t_{ox} is the oxide thickness, and $V_{th}(300K)$ and $V_{th}(77K)$ are the (measured) room-temperature and liquid-nitrogen threshold voltages.

Device		LW $(\mu m)^2$	N_d 10^{16} $(cm)^{-3}$	N_a 10^{16} $(cm)^{-3}$	t_{ox} nm	V_{th} (300K) V	V_{th}(77K) V
W10	N7	3 x 16	0.27	4.0	32	0.98 ± 0.05	1.48 ± 0.05
	P7	3 x 16	0.27	0.0	32	-1.35 ± 0.05	-1.70 ± 0.05
W44	NL	3 x 16	0.27	4.0	60	1.47 ± 0.05	2.15 ± 0.10
	PL	3 x 16	0.27	0.0	60	-1.46 ± 0.05	-1.99 ± 0.05

Noise measurements were performed on devices biased with constant gate-voltage, V_g, and drain current, I_d. A block diagram of the measurement circuit is shown in Figure 1 below. The gate-voltage was supplied directly, and the drain current indirectly (through a large ballast resistor R_B = 100 kΩ), by an HP-4140B dual voltage source/picoammeter. The devices, encapsulated in ceramic, 24-pin DIP packages, were mounted on a copper stage of an RMC-Cryosystems constant-flow liquid helium cryostat. Two silicon diode temperature sensors and a resistive heater were also attached to the copper stage. Stage temperature was monitored and controlled with a LakeShore Cryotronics model 330

temperature controller. A versatile junction box at the top of the cryostat allowed wiring to be changed for the various types of measurements. The MOSFET source and drain leads were connected (in parallel) to two EG&G PAR-113 low-noise amplifiers and a PAR-124A lock-in amplifier. One PAR-113 was dc-coupled to the device and had a voltage gain of 10. Its output was connected to one channel of a Keithley model 199 digital multimeter/scanner for measuring V_d. The second PAR-113 was ac-coupled to the device with a low-frequency cutoff of 30 mHz and a voltage gain of 10^4. Its output was fed into an HP-3562A dynamic signal analyzer, which was used to determine the power spectral density, $S_{V_d}(f)$, of drain-voltage fluctuations for frequencies, f, between 3 Hz and 50 kHz. The cryostat and analog instruments were housed in a Lindgren RF-shielded room. The HP-3562A, HP-4140B, and Keithley-199 were each controlled by a personal computer over the General Purpose Instrument Bus (GPIB).

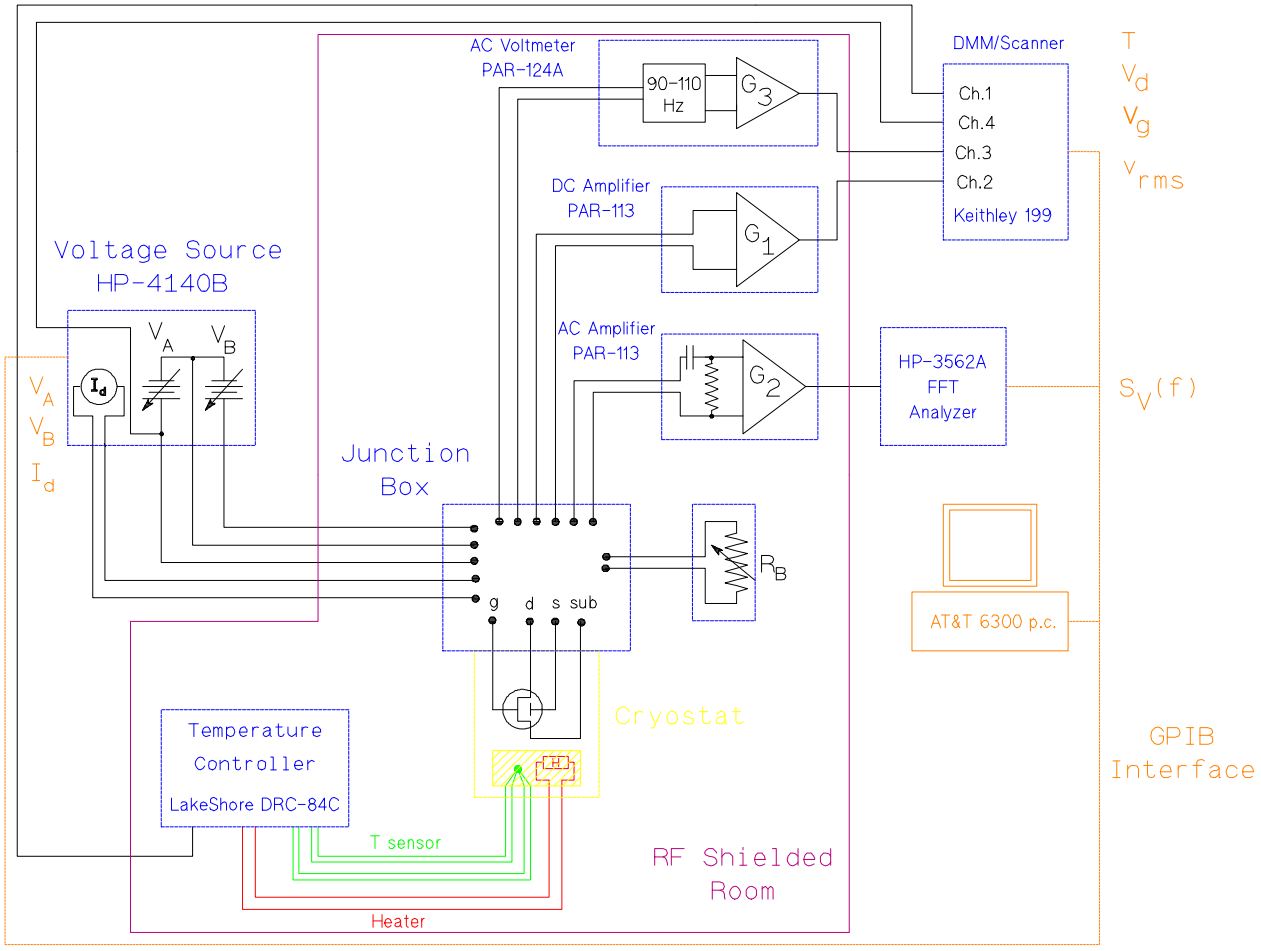

FIG. 1. Diagram showing the experimental setup.

The noise magnitude was conveniently characterized by recording the noise power in two different bandwidths which we refer to as the "narrow" (n) and "wide" (w) bandwidths. The PAR-124A lock-in amplifier was operated as a narrow band ac-voltmeter with a center frequency f_0 = 100 Hz and a bandwidth Δf = 14 Hz. Its output was connected to the dmm/scanner for recording v_n, where $(v_n)^2$ is the narrow band-limited noise power given by

$$(v_n)^2 \equiv \int_0^\infty |H(f)|^2 S_{V_d}(f)\,df \approx S_{V_d}(f_0)\Delta f\,, \qquad (2)$$

and H(f) is the transfer function of the ac-voltmeter. The wide band-limited noise power was obtained digitally by using the spectrum analyzer to integrate the noise spectrum between 5 and 50 Hz. This method gave $(v_w)^2$ given by

$$(v_w)^2 \equiv \int_{5Hz}^{50Hz} S_{V_d}(f)\,df\,. \qquad (3)$$

For pure 1/f noise we expect that the two are related by $v_w \approx 4.0\, v_n$. In practice, temperature scans of v_n and v_w showed slight differences owing to kinetic effects, i.e., spectral features that moved with temperature [7]. A typical room-temperature noise spectrum is shown in Figure 2.

To determine the gate-voltage dependence of the noise at fixed temperature, we initially measured v_n (with T and I_d

fixed) while slowly varying V_g over the range 100 mV ≤ $|V_g - V_{th}|$ ≤ 4 V. We discovered, however, that graphs of v_n/V_d versus V_g depended on the drain current. The problem was traced to the fact that, for any fixed I_d, the device did not remain in the linear regime for gate-voltages sufficiently close to threshold. We therefore modified our procedure to record measurements of v_n for a series of fixed V_g while scanning V_d. This method gave consistent results, but greatly complicated the data logging process. A more complicated gate-voltage dependence is observed when the device is not operated in the linear regime, presumably because of the non-uniform electric field along the channel [16, 20, 25].

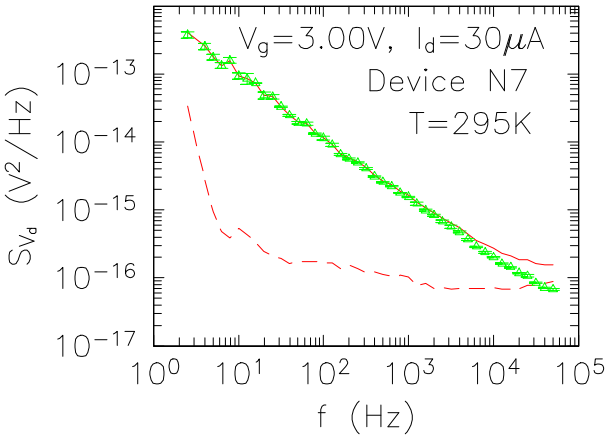

FIG. 2. Room temperature, drain-voltage noise spectrum for n-MOS device N7. The solid curve was measured with I_d = 30 μA and the dashed curve with I_d = 0. The symbols represent the "excess noise," i.e., with background subtracted.

The observed power spectral density of the drain-voltage fluctuations could be reasonably represented by

$$S_{V_d}(f, V_d) = \frac{A V_d^2}{f^{\gamma}} + S_{bg}(f), \qquad (4)$$

where the frequency exponent γ ≈ 1 and the background noise, $S_{bg}(f)$, due to device thermal noise and amplifier noise, was independent of the drain-voltage. Identifying the first term with the excess noise described above, we find that

$$(v_n)^2 \approx A\, V_d^2\, \frac{\Delta f}{f_0} + S_{bg}(f_0)\Delta f\,. \qquad (5)$$

Figure 3 shows graphs of the narrow band-limited noise power versus the square of the drain-voltage for this device for various gate-voltages at room temperature. Other devices behaved similarly. For sufficiently low V_d the expected linear behavior is observed. We note, however, that for V_d significantly greater than $0.1|V_g - V_{th}|$ the data deviate from linearity even though the I-V curves do not appear to deviate significantly from linearity. For instance, the trace for V_g=2.6V was terminated for V_d> 75 mV for this reason. Therefore, to ensure that values of v_n represent the noise in the linear regime, the noise amplitude $A(T,V_g)$ was determined from the slopes of these graphs as V_d approaches zero.

The temperature dependence of the noise was determined by measuring v_n for constant V_g and I_d while the sample was slowly cooled and/or heated between room and liquid nitrogen temperatures. First, detailed room-temperature measurements were performed for both the noise spectra and I-V curves, determining among other things, the threshold voltage, V_{th}(300K). Next, the device was biased in strong-inversion and cooled to 77 K over a period of roughly 30 minutes while recording V_d and v_n. At 77 K, the noise spectra and I-V curves were again measured, determining V_{th}(77K). Finally, the device was biased with fixed I_d and V_g and slowly heated to room temperature under computer control while continually logging V_d and v_n. The heating process took from 2-3 hours. Drain-voltage noise spectra for various temperatures were periodically measured and stored on the computer during the slow heating process. In all cases, data were reproducible after many days and heating/cooling cycles.

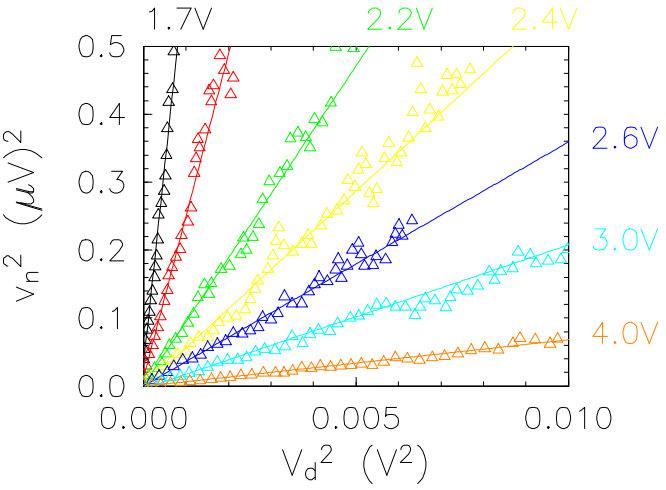

FIG. 3. Graphs of the room temperature, narrow band-limited noise power versus the square of the drain-voltage for device NL. The symbols represent data while the lines were obtained from unweighted linear least-squares fits.

The results of a typical temperature scan are shown in Figures 4 and 5. Figure 4 contains plots of the narrow and wide band-limited noise powers (left hand scale) and the drain-voltage (right hand scale) versus temperature. The solid squares are the measured $(v_n)^2$ while the open triangles are $(v_w)^2/16$. The two are expected to be identical for pure 1/f noise. The differences between the two band-limited noise power curves are associated with slight features in the frequency spectra of the noise. These are shown in Figure 5 which contains log-log plots of drain-voltage noise spectra versus frequency for a variety of

temperatures. Very slight deviations (i.e., structure) from 1/f noise is evident, with the structure "moving" to higher frequency with increasing temperatures. These kinetic effects have been neglected in this treatment but should be included in a more sophisticated model.

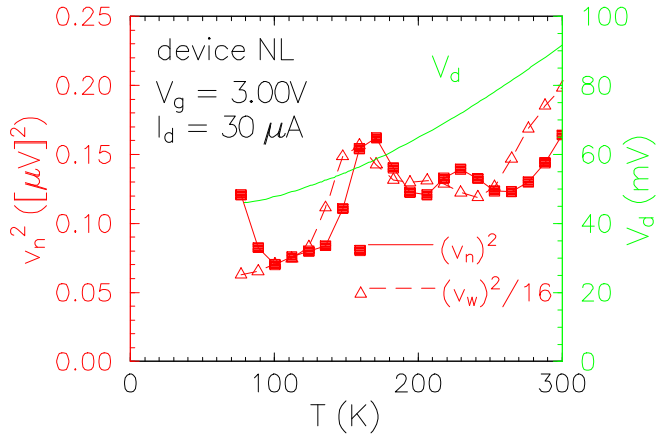

FIG. 4. Graphs of the narrow band-limited noise power (left hand scale) and drain-voltage (right hand scale) versus temperature for a typical n-MOS transistor. The solid squares were derived from measured v_n whereas the open triangles were derived from measured v_w.

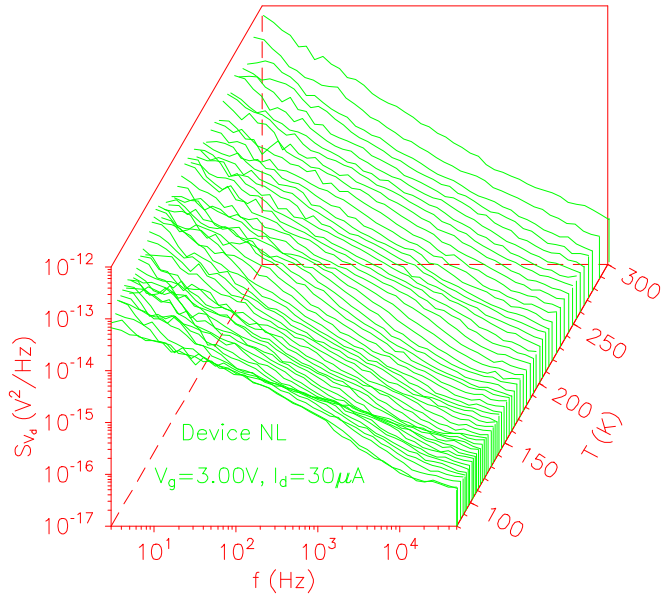

FIG. 5. Three-dimensional graph showing a series of noise spectra obtained at different temperatures for n-MOS device NL.

Experimental Results

Having described our method for determining the temperature- and gate-voltage dependencies of the 1/f noise of these devices, we now present the results. Figures 6 and 7 show plots of V_d/v_n for the room-temperature 1/f noise of n-MOS device NL and p-MOS device PL. Figure 6 clearly shows that, for the n-channel device, $v_n \propto V_d/(V_g - V_{th})$, consistent with Eq. (1) for a constant trap density, D_t. In contrast, Figure 7 shows a more complicated gate-voltage dependence for the noise of the p-MOS device.

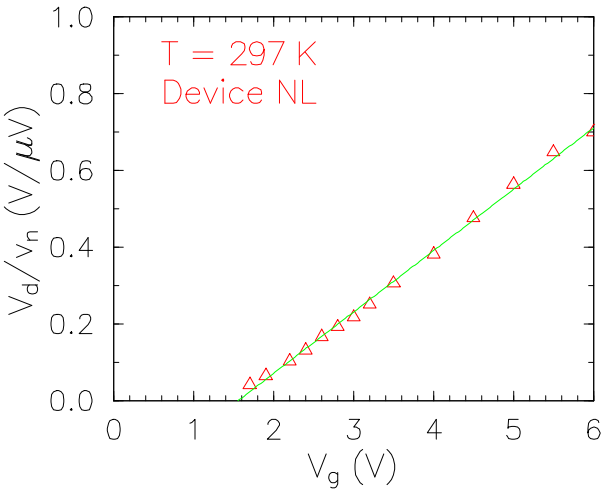

FIG. 6. Graph showing the room-temperature gate-voltage dependence of the 1/f noise for n-channel device NL, typical of that found for n-MOS devices. The symbols are data and the line is a least-squares fit to the data.

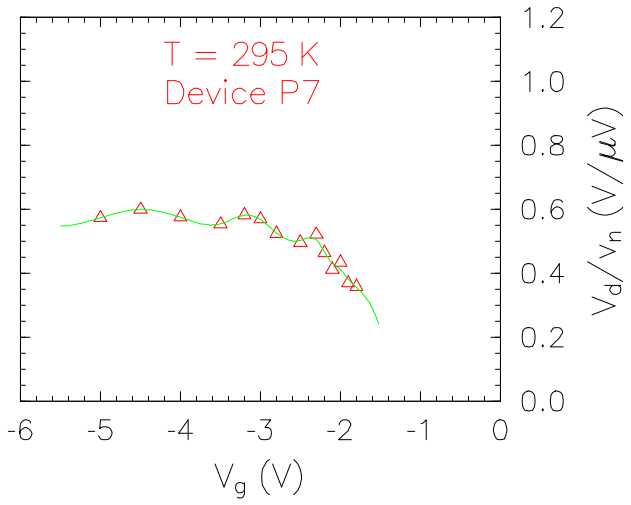

FIG. 7. Graph showing the room-temperature gate-voltage dependence of the 1/f noise for p-channel device P7. The symbols are data and the curve is a guide to the eye.

If the gate-voltage dependence of the room-temperature 1/f noise of p-MOS transistors arises from a non-uniform trap density, $D_t(E)$, then it should show up both in the V_g- and T-dependence of the noise. The reasoning is as follows. Only traps near the Si/SiO_2 interface and within a few kT of the quasi-fermi level communicate with the silicon [6, 9]. The fermi level changes with temperature while the trap energy levels move (relative to the fermi level) with gate-voltage. With a uniform trap density, the number of traps contributing to the noise at any V_g or T increases linearly

with T, but is otherwise independent of V_g and T, because D_t is a constant. This suggests that we look at the temperature dependence of the noise for the p-channel device P7 which shows the complicated gate-voltage dependence of the noise in Figure 7.

In order to directly compare the temperature and gate-voltage dependencies of the noise, it is useful to define an "excess" noise level K(T, V_g) that removes the expected drain-voltage and gate-voltage dependencies introduced through the transconductance.[1] Guided by Eq. (1), we define the 1/f noise level K(T,V_g) by [24]

$$K(V_g,T) \underset{\lim V_d \to 0}{\equiv} f\left\{S_{V_d}(f,V_d,V_g,T) - S_{V_d}(f,0,V_g,T)\right\}\frac{(V_g - V_{th})^2}{V_d^2} \quad (6)$$

We expect to find K independent of V_g and increasing linearly with T for 1/f noise due to trapping with an energy-independent trap density. If instead D_t is not constant, then a graph of K/T versus T should indicate the energy-dependence of the trap density, as the fermi level changes with temperature.

Figure 8 shows K/T for p-channel device P7.[2] Note that K/T increases rapidly with T near room temperature, suggesting that $D_t(E)$ is not constant, but rather, increases rapidly as E approaches the valence band edge. Figure 9 is the analogous plot for n-channel device NL. In contrast to what was observed for p-channel device, K/T for this device is nearly constant near room temperature, consistent with a constant D_t (for the relevant range of E) and with the observed gate-voltage dependence of the noise.

The gate-voltage dependence of K/T may similarly be used to map out the energy-dependence of the trap density. Figure 10 shows the gate-voltage dependence of K/T for n-channel device NL, again, confirming the constancy of the trap density. K/T varies by no more than 10% over the entire range of V_g, except for V_g very near threshold, where uncertainties are large.[3] Figures 9 and 10 are therefore consistent with each other, and both suggest that that the trap distribution is nearly constant near the conduction band edge.

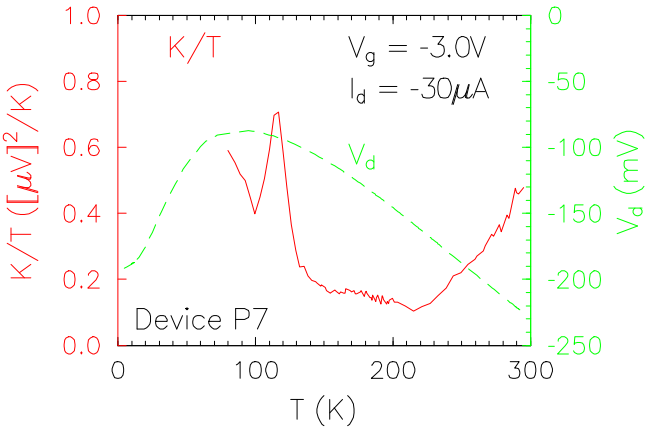

FIG. 8. Temperature dependence of the noise magnitude K/T (solid curve) and drain-voltage (dashed curve) for p-channel device P7.

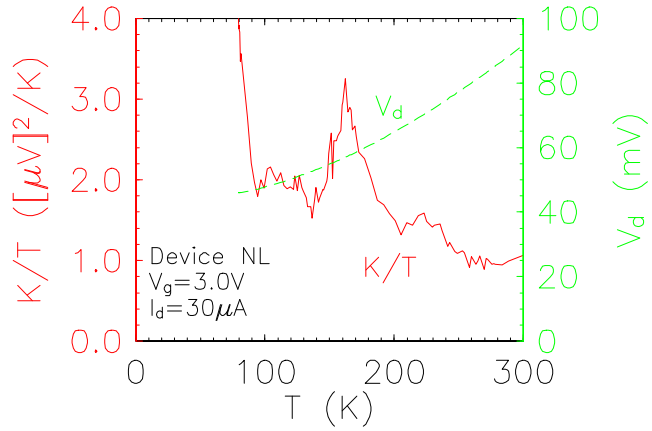

FIG. 9. Temperature dependence of the noise magnitude K/T (solid curve) and drain-voltage (dashed curve) for n-channel device NL.

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[1] This is equivalent to the practice, followed by many researchers, of referring the noise to the gate, i.e., calculating the spectrum of the apparent fluctuation in gate voltage. Note that, except for pure 1/f noise, K must also depend on frequency. Here we ignore any deviations from a 1/f frequency dependence (all of which were small) and assume that K may be calculated from either v_n, v_w, or S_{V_d} at any frequency.

[2] Here, K is calculated from the wide band-limited noise, v_w, since v_n was not logged during the temperature scans for this device.

[3] The dominant uncertainty in K/T is due to a±50 mV uncertainty in the threshold voltage, which leads to relatively large uncertainties in K/T near threshold. Moreover, calculated values of K suffer from a systematic error which is negligible when $R_{ch} << R_B$, but which becomes important near threshold. The systematic error may be removed by multiplying values presented by the factor $(R_B+R_{ch})^2/R_B^2$ which is as large as 1.3 for V_g = 1.7 V. The correction is less than 10% for $|V_g-V_{th}| > 400$ mV, and therefore does not affect any conclusions here.

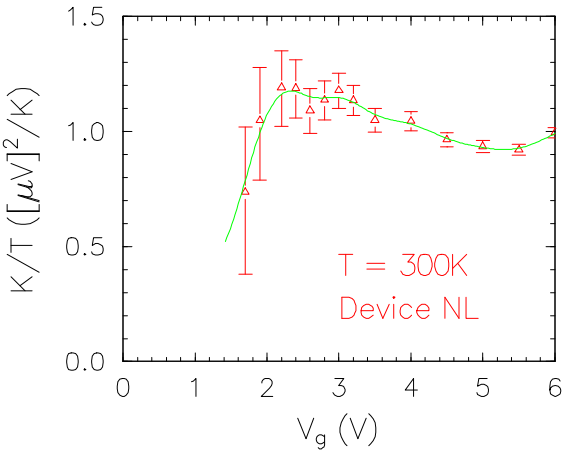

FIG. 10. Gate-voltage dependence of K/T for n-channel device NL near room temperature indicating a nearly energy-independent trap density, D_t. The curve is a guide to the eye.

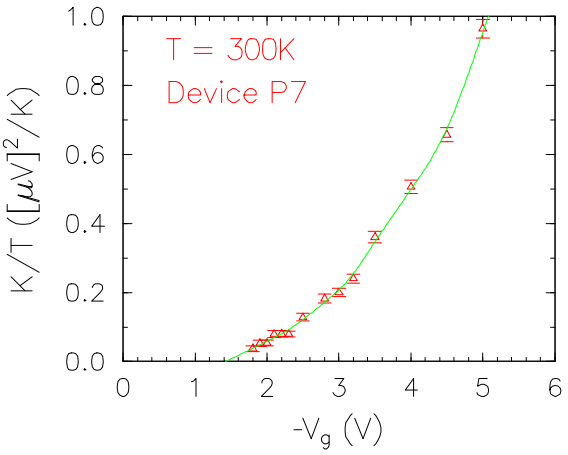

FIG. 11. Gate-voltage dependence of K/T for p-channel device P7 near room temperature, indicating a strong energy-dependence to the trap density, $D_t(E)$. The curve is a guide to the eye.

Figure 11 shows the gate-voltage dependence of K/T for p-channel device P7. In contrast to the above result, here K/T varies by nearly two orders of magnitude over the range of V_g! Figures 8 and 11 are consistent with each other and both suggest that the trap distribution varies strongly with energy near the valence band edge.[4]

To take this picture one step further, Figure 8 suggests that the trap density for device P7 is relatively flat for energies corresponding to temperatures between 140K and 220K and V_g = -3.0 V. A graph of K/T versus V_g (not shown) for measurements at T = 175 K confirms this, and a graph of V_d/v_n versus V_g (also not shown) looks similar to Figure 6, as expected.

Data from p-MOS transistor PL illustrates these ideas best, not because the device behaves any differently from the others, but simply because a more complete data set was recorded for this device. Figure 12 shows K/T calculated from a temperature-scan of the narrow band-limited noise power measured for fixed V_g = -3.0V. The solid curve represents K/T (left hand scale) while the dashed curve represents V_d (right hand scale). Four features, labeled A (280K), B (200K), C (130K), and D (90K), are identified in the trap density (i.e., K/T). Figures 13-15 show K/T as determined from gate-voltage scans of the narrow band-limited noise power at fixed temperatures, T = 300K, 137K, and 80K respectively. These gate-voltage scans show the same features in the trap density. Feature A is found in the gate-voltage scan performed at T = 300 K, C and B in the 137 K scan, and D and C in the 80 K scan. The features are very distinctive at lower temperatures

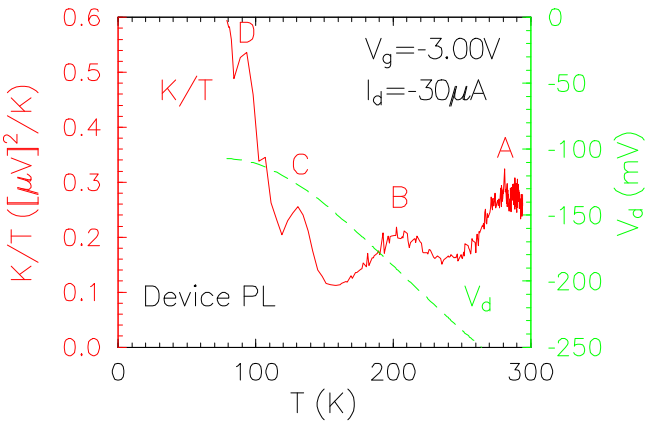

FIG. 12. Temperature dependence of the noise magnitude K/T (solid curve) and drain-voltage (dashed curve) for device PL. Four peaks A, B, C, and D are identified for reference to later figures.

where k_bT is small and less distinctive at higher temperatures where k_bT gets broader.

[4] Note that there is slight disagreement between the two figures as to the value of K(T, V_g) at T = 300 K and V_g = -3.00V. This disagreement comes from the fact that for the temperature scan K is calculated from v_w and for the gate-voltage scan K is calculated from v_n. For other devices where K/T was always calculated from v_n there is no discrepancy.

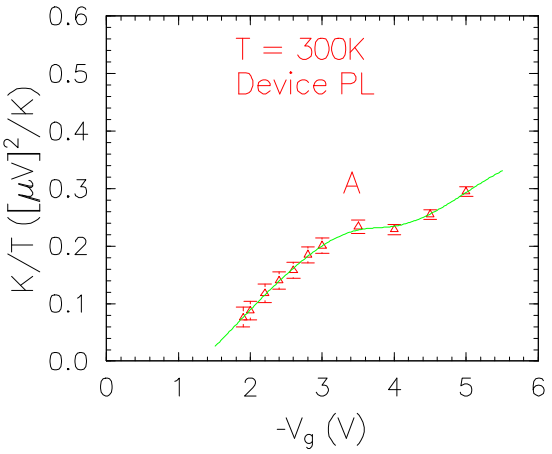

FIG. 13. Gate-voltage dependence of K/T for p-channel device PL at room temperature. The curve is a guide to the eye. The location of peak "A" is identified in the trace.

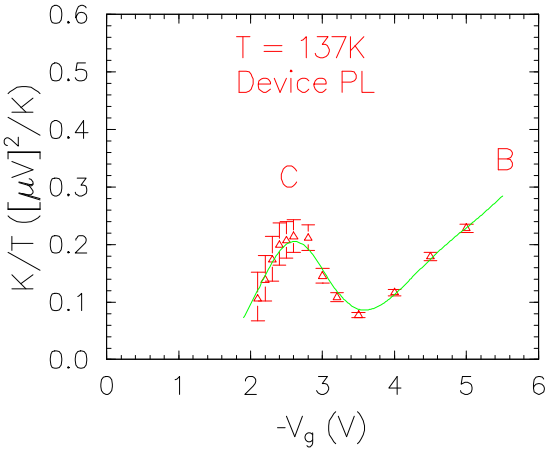

FIG. 14. Gate-voltage dependence of K/T for p-channel device PL at T = 137 K. The curve is a guide to the eye. The locations of peaks C and D are identified in the trace

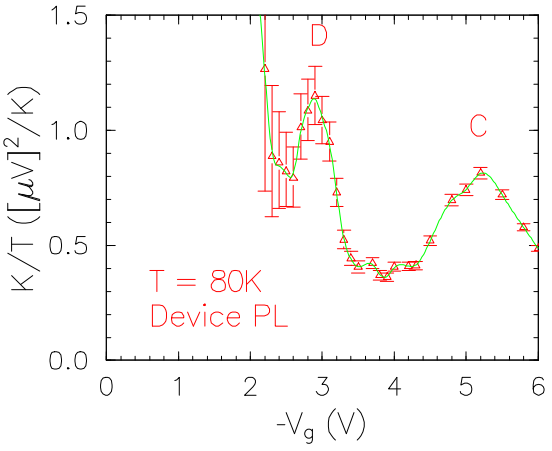

FIG. 15. Gate-voltage dependence of K/T for p-channel device PL at T = 80 K. The curve is a guide to the eye. The locations of peaks C and D are identified in the trace.

Figures 12 and 13 suggest that, at room temperature, the gate-voltage dependence of the noise should be the simple dependence typically observed for n-channel devices. This is verified by measurements shown in Figure 16.

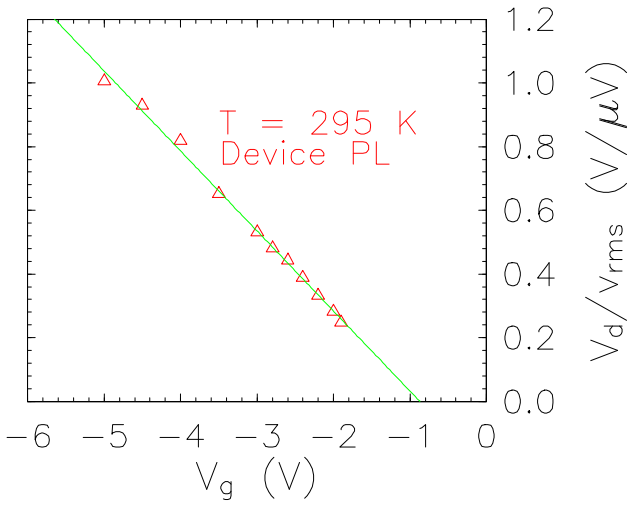

FIG. 16. Gate-voltage dependence of the room-temperature 1/f noise of p-channel device PL. Symbols represent data and the line is obtained from a linear least-squares fit to the data.

For completeness, we show the temperature dependence of K/T for n-MOS transistor N7 in Figure 17. Additional data may be found elsewhere [9]. As was the case for device NL, the data of Figure 17 indicate that $D_t(E)$ is nearly constant near room temperature, leading to the gate-voltage dependence usually observed for n-MOS transistors.

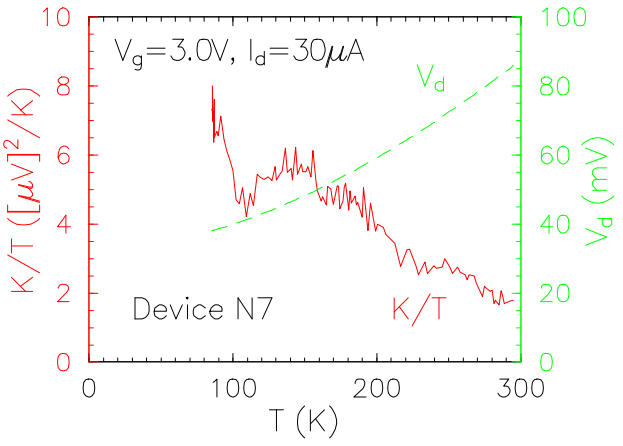

FIG. 17. Temperature dependence of the noise magnitude K/T (solid curve) and drain-voltage (dashed curve) for device N7.

Discussion

For some time it has been known that the 1/f noise of n-MOS and p-MOS transistors tend to show different gate-voltage dependencies [10]. Two schools of thought have emerged to explain these differences. One school of thought attributes the noise of n-MOS transistors and p-MOS transistors to two different mechanisms: a surface trapping

mechanism for n-MOS transistors and a bulk mobility fluctuation mechanism (i.e., Hooge model) for p-MOS transistors [11]. The second school of thought attributes the noise of both n-MOS and p-MOS transistors to trapping, with the trap density constant for n-MOS transistors and varying with gate-voltage for p-MOS transistors [10, 12]. Our data support this latter viewpoint and support a natural explanation for the gate-voltage dependence of D_t. Both schools of thought can explain the observed gate-voltage dependence of the noise. We believe, however, that the trapping model offers a clear and simple explanation for the observed T-dependence and relationship between the T- and V_g-dependence of the noise.

Other measurements of the gate-voltage dependence of the 1/f noise of either p-MOS or n-MOS transistors [12, 13, 16, 17, 20, 26, 27], and measurements of the T-dependence of the noise of either n-MOS or p-MOS [14, 15, 21] devices are reported in the literature. In a few cases researchers report limited data on both V_g- and T-dependence [14, 15]. These generally appear to be consistent with the results presented here. For instance, Chang et al. [15] have recently reported $S_{V_d} \propto V_d^2/(V_g-V_{th})^2$ for n-MOS transistors. For these same devices they find that the noise increases weakly with temperature. For the noise of p-MOS transistors they report a more complicated gate-voltage dependence, and a *decrease* in noise with *increasing* temperature. Wang et al. have performed noise and DLTS measurements on p-MOS transistors and conclude that $D_t(E)$ increases towards the valence band edge [17]. Abidi has investigated the V_g-dependence of the noise in p-MOS transistors and observed results similar to those reported here [12].

Due to the obvious gate-voltage dependence of the transconductance, the power spectral density of drain-voltage fluctuations associated with capture and emission of charge carriers is expected to vary as $S_{V_d} \propto V_d^2/(V_g-V_{th})^2$. Additional V_g-dependence is introduced by an energy-dependent trap density, $D_t(E)$. If D_t depends only weakly on E, then the gate-voltage dependence of S_{V_d} will be dominated by that of the transconductance. This is apparently the case for electron trap energies near the conduction band which are responsible for the room-temperature noise of n-channel MOSFETs operated in strong inversion. If instead, D_t varies strongly with trap energy, the gate-voltage dependence of S_{V_d} will be more complicated, and, depending upon the nature of $D_t(E)$, might vary with V_g either more or less strongly than does the transconductance. Apparently there is a tendency for the density of hole trap energies to increase rapidly as E moves away from midgap and into the valence band (increasing hole energy), as indicated by the room-temperature noise of p-channel MOSFETs. The "peak" features in our graphs of K/T suggest that there are several well-defined trap levels that contribute to the noise of our devices.

We have used graphs of K/T versus T and K/T versus V_g to *qualitatively* describe the energy dependence of the trap density. Increasing temperature and increasing gate-voltage magnitude (i.e., towards stronger inversion) cause the trap energy responsible for the noise to move away from midgap and into the relevant band (conduction band for n-channel and valence band for p-channel devices). In principle, the data may be used to *quantitatively* extract $D_t(E)$. To accomplish this, one must solve Poisson's equation for the band-bending, $\psi(x)$, to obtain the surface potential, ψ_s for various combinations of T and V_g. Others have used this approach to extract $D_t(E_t)$ from noise measurements in MOSFETs [21, 26, 28-30]. This problem is readily solved using Boltzmann statistics, relevant for weak inversion and high temperatures [31]. For our measurements these calculations need to be performed using Fermi-Dirac statistics, greatly complicating the problem. This represents an obvious direction for future work. Our data indicate several well-defined peaks in K/T which may be associated with dominant trapping levels. With a quantitative trap energy scale it might be possible to relate these defects to other known properties of these devices. For example, with noise measurements it may be possible to map the energy dependence of "border traps" (near-interfacial oxide traps which communicate with the Si [32, 33]) in much the same way as C-V or conductance measurements are used to map interface-trap densities [31].

The discussion above clearly leaves out a number of important physical features which must be considered in developing a comprehensive understanding of trapping noise in MOSFETs, even when restricted to device operation in strong inversion in the linear regime. A more complete model, for instance, must allow for the kinetic effects associated with changes in temperature (i.e., the speeding up and slowing down of capture and/or emission), not just the static effects associated with the trap density at the fermi level. Also, the effects of variation of the trap density, $D_t(E,x)$, with depth into the oxide should be considered [28]. Moreover, measurements of random telegraph signals in small channel MOSFETs indicate that traps are not uniquely identified with a single trap energy, as trap capture and/or emission of a charge carrier may be associated with lattice relaxation [1]. Finally, there are also changes in scattering cross-sections of traps which change charge states during capture and emission events that will lead to correlated number and mobility fluctuations [26, 29].

Conclusions

We have investigated the temperature and gate-voltage dependence of the 1/f noise of p-channel and n-channel MOS transistors on the same chips. We find a correlation between these two dependencies which may be qualitatively explained in terms of an energy-dependent trap density, $D_t(E)$. For our n-channel transistors we find that D_t tends to be only weakly dependent on trap energy in the range of E typically accessed with room temperature operation in strong inversion. This leads to a drain-voltage noise

spectrum that varies inversely with $(V_g-V_{th})^2$ and increases approximately linearly with T. This appears to be consistent with other data in the literature. For our p-channel transistors we find that D_t varies strongly with trap energy for similar temperature and device operating conditions, increasing rapidly as E moves (away from midgap) into the valence band. This too appears to be consistent with data in the literature. At lower temperatures the temperature dependence of the p-MOS noise can be less strong. In these regions of weak temperature variation, the noise varies inversely with $(V_g-V_{th})^2$, consistent with a simple trapping model of the noise. We conclude that variations in $D_t(E)$ can account for much, if not all, of the discrepancy typically observed in the gate-voltage dependence of the room-temperature 1/f noise of n- and p-MOS transistors.

Acknowledgments

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[1] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: a new perspective on individual defects, interface states, and low-frequency (1/f) noise," *Adv. in Phys.***38**, 367-468 (1989).

[2] D. M. Fleetwood and J. H. Scofield, "Evidence that similar point defects cause 1/f noise and radiation-induced-hole trapping in metal-oxide-semiconductor transistors," *Phys. Rev. Lett.* **64**, 579-82 (1990).

[3] K. S. Ralls, W. J. Skocpol, L. D. Jackel, R. E. Howard, L. A. Fetter, R. W. Epworth, and D. M. Tennant, "Discrete resistance switching in submicrometer silicon inversion layers: individual interface traps and low-frequency (1/f?) noise," *Phys. Rev. Lett.* **52**, 228-31 (1984).

[4] A. van der Ziel, "On the noise spectra of semi-conductor noise and of flicker effect," *Physica* **15**, 359-72 (1957).

[5] F. K. duPre, "A suggestion regarding the spectral density of flicker noise," *Physical Review* **78**, 615 (1950).

[6] A. L. McWhorter, "1/f noise and germanium surface properties," in *Semiconductor Surface Physics* (University of Pennsylvania Press, Philadelphia, 1957), pp. 207-228.

[7] P. Dutta and P. M. Horn, "Low-frequency fluctuations in solids: 1/f noise," *Rev. Mod. Phys.* **53**, 497 (1981).

[8] J. J. Simonne, G. Blasquez, and G. Barbottin, "1/f noise in MOSFETs," in *Instabilities in Silicon Devices: Silicon Passivation and Related Instabilities, Vol. 2,* (Elsevier, Amsterdam, 1989), pp.639-57.

[9] J. H. Scofield and D. M. Fleetwood, "Physical basis for nondestructive tests of MOS radiation hardness," *IEEE Trans. Nucl. Sci.* **NS-38**, 1567-77 (1991).

[10] A. van der Ziel, "Flicker noise in electronic devices," in *Advances in Electronics and Electron Physics, Vol. 49,* edited by Martin and Martin (Academic Press, New York, 1979), pp. 225-297.

[11] L. K. J. Vandamme and Xiaosong Li, "1/f noise in MOS transistors due to number or mobility fluctuations," in *Noise in Physical Systems and 1/f Fluctuations, AIP Conference Proceedings, Vol. 285,* edited by P. H. Handel and A. L. Chung (American Institute of Physics, New York, 1993), pp.345-53.

[12] A. A. Abidi, C. R. Viswanathan, J. Chang, J. J.-M. Wat, and J. A. Wikstrom, "Uniformity in flicker noise characteristics of CMOS IC technologies," in *Proc. 9th Int. Conf. on Noise in Physical Systems,* ed. C. M. Van Vliet (World Scientific, Singapore, 1987), pp.469-72.

[13] J. Chang and C. R. Viswanathan, "Low-frequency noise in CMOSTs at cryogenic temperatures," in *Proc. 10th Int. Conf. on Noise in Physical Systems, 1989, Budapest, Hungary,* edited by A. Ambrozy (Akademiai Kiado, Budapest, 1990), pp.499-502.

[14] J. Chang and C. R. Viswanathan, "Flicker noise in CMOS transistors - a one dimensional numerical model,"in *Noise in Physical Systems and 1/f Fluctuations,* ed. T. Musha, S. Sato, and M. Yamamoto (Ohmsha, Ltd., Tokyo, 1991), pp. 245-8.

[15] J. Chang and C. R. Viswanathan, "Modeling and characterization of flicker noise in CMOS transistors from subthreshold to strong inversion," in *Noise in Physical Systems and 1/f Fluctuations, AIP Conference Proceedings, Vol. 285,* edited by P. H. Handel and A. L. Chung (American Institute of Physics, New York, 1993), pp.358-61.

[16] H. Wong and Y. C. Cheng, "Gate dielectric-dependent flicker noise in metal-oxide-semiconductor transistors," *J. Appl. Phys.* **67**, 478-84 (1978).

[17] K. L. Wang, "Measurements of residual defects and 1/f noise in ion-implanted p-channel MOSFET's," *IEEE Trans. Elec. Dev.* **ED-25**, 863-7 (1990).

[18] D. M. Fleetwood and N. Giordano, "Direct link between 1/f noise and defects in metal films," *Phys. Rev. B* **31**, 1157-1160 (1985).

[19] J. H. Scofield, J. V. Mantese, and W. W. Webb, "Temperature dependence of noise processes in metals," *Phys. Rev. B* **34**, 723-731 (1986).

[20] Z. Celik and T. Y. Hsiang, "Study of 1/f noise in n-MOSFETs: linear regime," *IEEE Trans. Electron. Dev.* **ED-32**, 2797-801 (1985).

[21] Z. Celik-Butler and T. Y. Hsiang, "Determination of $Si:SiO_2$ interface trap density by 1/f noise measurements," *IEEE Trans. Elec. Dev.* **ED-35**, 1651-1655 (1988).

[22] D. Vuillaume, "Comments on 'Determination of $Si:SiO_2$ interface trap density by 1/f noise measurements,'" *IEEE Trans. Elec. Dev.* **ED-37**, 824-5 (1990).

[23] Z. Celik-Butler and T. Y. Hsiang, "Reply to 'comment on "Determination of $Si:SiO_2$ interface trap density by 1/f noise measurements,"'" *IEEE Trans. Elec. Dev.* **ED-37**, 825-6 (1990).

[24] J. H. Scofield, T. P. Doerr, and D. M. Fleetwood, "Correlation between preirradiation 1/f noise and postirradiation oxide-trapped charge in MOS transistors," *IEEE Trans. Nucl. Sci.* **NS-36**, 1946-1953 (1989).

[25] H. Mikoshiba, "1/f noise in n-channel silicon-gate MOS transistors," *IEEE Trans. Elec. Dev.* **ED-29**, 965-70 (1982).

[26] C. Surya and T. Y. Hsiang, "Theory and experiment on the $1/f^{\gamma}$ noise in p-channel metal-oxide-semiconductor field-effect transistors at low drain bias," *Phys. Rev. B* **33**, 4898-4905 (1986).

[27] C. T. Sah and F. H. Hielscher, "Evidence of the surface origin of the 1/f noise," *Phys. Rev. Lett.* **17**, 956-958 (1966).

[28] Z. Celik-Butler and T. Y. Hsiang, "Spectral dependence of 1/f^γ noise on gate bias in n-MOSFETs," *Sol.-State Electron.* **30**, 419-23 (1987).
[29] K. K. Hung, Ping K. Ko, Chenming Hu, and Yiu C. Cheng, "A unified model for the flicker noise in metal-oxide-semiconductor-field-effect transistors," *IEEE Trans. Elec. Dev.* **ED-37**, 654-65 (1990).
[30] O. Jantsch and B. Borchert, "Determination of interface state density especially at the band edges by noise measurements on MOSFETs," *Sol. St. Electron.* **30**, 1013-15 (1987).
[31] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, (John Wiley \& Sons, Inc., New York, 1982).
[32] D. M. Fleetwood, "Border traps in MOS devices," *IEEE Trans. Nucl. Sci.* **NS-39**, 269-271 (1992).
[33] D. M. Fleetwood, P. S. Winokur, R. A. Reber, Jr., T. L. Meisenheimer, J. R. Schwank, M. R. Shaneyfelt, and L. C. Riewe, "Effects of oxide traps, interface traps, and 'border traps' on MOS devices," *J. Appl. Phys.* **73**, 5058-74 (1993).